GR551x Errata Note

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Preface

Purpose

This document lists application limitations and relevant workarounds for GR551x System-on-Chip (SoC) series, aiming at helping users fully understand and better use the SoC series.

Audience

This document is intended for:

- GR551x user
- GR551x developer
- GR551x tester
- Hobbyist developer

Release Notes

This document is the second release of *GR551x Errata Note*, corresponding to GR551x SoC series.

Revision History

Version	Date	Description
1.0	2021-06-01	Initial release
1.1	2021-09-09	• Changed “Conditions” to “Cause” in all sections. • Optimized descriptions in “PMU”, “ADC”, “Calendar”, “SPI”, and “QSPI” sections.

Contents

1 GR551x Usage Limitations

This chapter lists possible issues due to design limitations, analyzes causes and impact, as well as provides recommended workarounds for users during product development based on GR551x System-on-Chips (SoCs), helping them give full play to the performance of GR551x SoCs under these limitations.

1.1 PMU

1.1.1 Abnormally High Power Consumption for GR5515I0ND and GR5515I0NDA in Sleep Mode

- Description

  For GR5515I0ND and GR5515I0NDA that require external Flash, the internal IO LDO of the SoC is used to supply power to external Flash. Relatively small voltage drop (< 100 mA) between VBATL and IO LDO results in electricity leakage which leads to abnormally high power consumption for the SoC.

- Cause

  Electricity leakage is caused due to internal pin status design of the SoC when the voltage drop between VBATL and IO LDO is lower than 100 mA.

- Impact

  The SoC power consumption is abnormally high in sleep mode.

- Recommended Workaround

  In application scenarios where the VBATL voltage is close to that provided by the IO LDO (voltage drop < 100 mV), you shall connect VIO_LDO_OUT to VBATL and supply the Flash via VBATL. The following two recommended workarounds are provided to adapt to different application scenarios:

  - For GR5515I0ND or GR5515I0NDA that requires 3.3 V external Flash and the VBATL supply voltage is 3.3 V, connect VIO_LDO_OUT to VBATL on the SoC during hardware design. DO NOT use the internal IO LDO of the SoC to supply the external Flash.
  - For GR5515I0NDA that requires 1.8 V external Flash and the VBATL supply voltage is 3.3 V, use the internal IO LDO of the SoC to supply the external Flash.

Note:

The recommended workaround is available on GR551x SDK V1.6.06 and later versions.

1.2 ADC

1.2.1 ADC Measurement Error Due to Non-Compliant SoC Supply Voltage When Internal Reference Source Is Used

- Description

  For ADC with an internal reference source (voltage value: 1P2V or 1P6V), a large ADC measurement error occurs, leading to failure to meet customer measurement requirements.

- Cause

  The maximum voltage for internal modules within a GR551x SoC is determined by VBATL. If the internal reference voltage of the ADC is higher than the VBATL value, the ADC fails to work normally because the SoC cannot provide the accurate reference voltage required by the ADC.

- Impact

  The SoC fails to supply a voltage that meets the internal reference source level required by the ADC, resulting in a non-compliant reference voltage that leads to a large ADC measurement error.

- Recommended Workarounds

  Different reference voltage values require different SoC supply voltages. To achieve optimal ADC performance and decrease the ADC measurement error, ensure the SoC supply voltage is within the reference range listed in the table below:

Table 1-1 Reference range of SoC supply voltage specific to reference sources

Reference Source	Range of SoC Supply Voltage
0P8V	2.1 V–3.8 V
1P2V	2.6 V–3.8 V
1P6V	3.2 V–3.8 V

1.3 Calendar

1.3.1 Calendar Partially Functions Abnormally

- Description

  When the internal RC clock is used as the slow-speed system clock, the calendar calibration fails, and the Calendar module cannot work properly.

- Cause

  During hardware design, the Calendar module is not expected to support using the internal RC clock as the clock source.

- Impact

  There is no clock input, so calendar calibration fails, and the Calendar module cannot work properly.

- Recommended Workaround

  Note that when the internal RC clock is chosen (in *custom_config.h*) as the slow-speed system clock, both the app_rtc and alarm cannot work properly. To avoid this limitation, you can choose 32K RTC as the slow-speed system clock.

Note:

The recommended workaround is available on GR551x SDK V1.6.06 and later versions.

1.4 SPI

1.4.1 Transfer Rate of HAL SPI cannot Reach 32 MHz When CS Pins Are Controlled by Hardware

- Description

  When the HAL SPI module transfers data in DMA mode, the transfer rate cannot reach 32 MHz if CS pins are controlled by hardware (SPI module).

- Cause

  Due to IP design limitations, data in SPI TX FIFO may be consumed to empty when internal modules within a GR551x system compete for bus resources. In this case, the SPI controller automatically releases CS signals which lead to timing disorder of SPI transmission during SPI TX FIFO reloading.

- Impact

  A data transfer error occurs.

- Recommended Workaround

  Do not control CS pins through hardware. Instead, utilize PIN_MUX registers to configure the CS pins as GPIO pins, and then use software to drive the pins to implement chip select functionality (CS controlled by software). In this case, the SPI module transfers data in DMA mode at 32-bit data width and up to 32 MHz transfer rate.

Note:

This workaround has been integrated into GR551x SDK V1.6.06 or later at the driver layer of applications to control CS by software.

1.5 QSPI

1.5.1 QSPI Encounters Abnormalities During Data Transfer at 32 MHz

- Description

  In both polling and interrupt modes, the QSPI module fails to transfer data at a rate of 32 MHz.

  In DMA mode at 8-bit or 16-bit data width, the QSPI module fails to transfer data at a rate of 32 MHz.

- Cause

  This abnormality occurs due to relevant IP design limitations. In interrupt or DMA mode, data in QSPI TX FIFO may be consumed to empty without in-time loading of new data when the MCU is inefficient in processing tasks or internal modules within a GR551x system compete for bus resources. In this case, the QSPI controller automatically releases CS signals which lead to timing disorder of QSPI transmission during QSPI TX FIFO reloading. During data reception in DMA mode, when data in QSPI RX FIFO cannot be migrated to SRAM in time due to internal competition for bus resources, RX FIFO overflow occurs, followed by failure to receive data for the QSPI controller.

- Impact

  A transfer abnormality occurs, and correct data cannot be obtained.

- Recommended Workaround

  To ensure stable data transfer for QSPI module, choose DMA mode and set a proper transfer rate according to data width. Recommended transfer rates are listed as below:

Table 1-2 QSPI transfer rates specific to data width

Data Width	Transfer Rate	QSPI Data Transfer in DMA Mode
8 bits	8 MHz	Successful
16 bits	16 MHz	Successful
32 bits	32 MHz	Successful

Note:

The GR551x QSPI module transfers data in big-endian order while the GR551x system bus adopts little-endian order, resulting in reverse orders of transferred data bytes. Therefore, data processing at the application layer is required.

1.5.2 Mode1 and Mode3 Are Unavailable in Non-Single QSPI Modes

- Description

  Both Mode1 and Mode3 for the QSPI module are unavailable in non-single (dual-SPI and quad-SPI) modes.

- Cause

  This abnormality occurs due to relevant IP design limitations.

- Impact

  A transfer abnormality occurs, and correct data cannot be obtained.

- Recommended Workaround

  Adopt Mode0 or Mode2 for dual-SPI or quad-SPI data transfer.

Note:

Mode 0, Mode1, Mode2, and Mode 3, as four standard clock modes for the QSPI module, are used to configure clock edges and phases for the module.