TFA9872_SDS

High Efficiency Class-D Audio Amplifier with Speaker-as-Microphone

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Contents

1 General description

The TFA9872 is a 9.5 V boosted class-D audio amplifier featuring Speaker-as-Microphone (SaM) and Receiver-as-Microphone (RaM) modes. It can deliver up to 10.0 W peak output power into an 8 Ω speaker and up to 11.8 W peak output power into a 6 Ω speaker, at a supply voltage of 4.0 V. The internal adaptive DC-to-DC converter raises the supply voltage to 9.5 V, providing ample headroom for major improvements in sound quality.

Internal adaptive DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary, maximizing the output power of the class-D audio amplifier while limiting quiescent power consumption.

The device can be configured to drive either a hands-free speaker (4 Ω to 8 Ω) for audio playback, or a receiver speaker (32 Ω) for handset playback, allowing it to be embedded in platforms that support either or both options. The maximum output power, gain, and noise levels are lower in the Handset Call use case than in the Hands-free Call use case.

The SaM feature allows the speaker to be used as an additional microphone when not configured for audio playback. This function performs best in high sound pressure environments (like concert recording or wind noise calls) and is targeted at such use cases.

The TFA9872 also incorporates battery protection. By limiting the supply current when the battery voltage is low, the device is prevented from switching off unexpectedly due to excessive load currents (excessive load currents can lead to a system undervoltage).

Because it has a digital input interface, the TFA9872 features low RF susceptibility. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The audio input interface is I^2S and the control settings are communicated via an I^2C-bus interface.

The TFA9872 is available in a 42-bump WLCSP (Wafer Level Chip-Size Package) with a 400 mm pitch.

2 Features and benefits

- High output power: 5.1 W (average) into 8 W at 4.0 V supply voltage (THD = 1 %)
- Supports handset (16 Ω or 32 Ω) and hands-free (4 Ω or 8 Ω) speaker configurations
- High efficiency, low power dissipation and low-noise speaker driver
- Adaptive DC-to-DC converter increases the supply voltage smoothly when switching between fixed boost and adaptive boost modes, preventing large battery supply spikes and limiting quiescent power consumption.
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Very low noise output <20×mV (with null data input at F_s = 48 kHz)
- Low battery current consumption <130 mA (P_o = 380 mW, average music power)
- I^2C-bus control interface (400 kHz)
- Speaker current and voltage monitoring (via the I^2S-bus) for Acoustic Echo Cancellation (AEC) at the host
- 16 kHz /44.1 kHz/48 kHz sample frequencies supported
- Ultrasonic support (limited) via TDM/I^2S running at 96 kHz/192 kHz
- Configurable full-duplex 4-wire TDM/I^2S input interface supporting up to 16 slots
- Low-latency input path supporting side tone mixing via dedicated PDM input interface
- Speaker-as-Microphone feedback path on dedicated PDM output interface or TDM interface
- Programmable interrupt control via a dedicated interrupt pin
- Low RF susceptibility
- Thermal foldback and overtemperature protection
- 15 kV system-level ESD protection without external components on amplifier output

3 Applications

- Mobile phones & Tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- Internet of Things applications embedding high-quality audio

4 Quick reference data

Table 4-1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT V_{BAT} must not be lower than V_{DDD} or V_{DDE} in application	2.7	-	5.5	V
V_{DDD}	digital supply voltage	on pin VDDD	1.65	1.8	1.95	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDE	1.65	1.8	1.95	V
I_{BAT}	battery supply current	Active state on pin VBAT; Operating mode with load; R_L = 6 Ω; DC-to-DC converter in Adaptive Boost mode; P_o = 380 mW (average music power); V_{BAT} = 4.0 V; V_{DDP} = 8.5 V	-	122	-	mA
		Idle state on pin VBAT; Operating mode with load; R_L = 6 Ω and no output signal (idle); DC-to-DC converter in Adaptive Boost mode; V_{BAT} = 4.0 V; V_{DDP} = 8.5 V	-	1.8	-	mA
		Power-down state on pin VBAT; DC-to-DC converter in power-down mode; T_j = 25 °C; no clock	-	1	-	μA
I_{DDD}	digital supply current	Active state on pin VDDD; Operating mode with load; R_L =6 Ω; DC-to-DC converter in Adaptive Boost mode, P_o = 380 mW (average music power), V_{BAT} = 4.0 V; V_{DDP} = 8.5 V	-	6.8	-	mA
		Idle state on pin VDDD; Operating mode with load; R_L =6 Ω and no output signal (idle); DC-to-DC converter in Adaptive Boost mode; V_{BAT} = 4.0 V; V_{DDP} = 8.5 V	-	4.1	-	mA
		Power down state on pin VDDD; DC-to-DC converter in power-down mode; T_j = 25 °C; no clock	-	10	-	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{o(AV)}$	average output power	THD+N = 1 %; L_L = 44 µH; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V				
		V_{BST} = 9.5 V; R_L = 8 Ω	-	5.1	-	W
		V_{BST} = 8.5 V; R_L = 8 Ω	-	4.0	-	W
		V_{BST} = 9.5 V; R_L = 6 Ω	-	5.9	-	W
		V_{BST} = 8.5 V; R_L = 6 Ω	-	5.1	-	W
SaM S/N	speaker-as-microphone signal-to-noise ratio	A-weighted; PDM output; full scale input; PGA gain setting GAIN_10	-	78.6	-	dB

5 Ordering information

Table 5-1: Ordering information

Type number	Package		
	Name	Description	Version
TFA9872AUK/N1	WLCSP42	wafer level chip-scale package; 42 bumps; 3.13 × 2.46 × 0.50 mm	SOT1459-2
TFA9872CUK/N1	WLCSP42	wafer level chip-scale package; 42 bumps; 3.13 × 2.46 × 0.525 mm	SOT1459-2

6 Block diagram

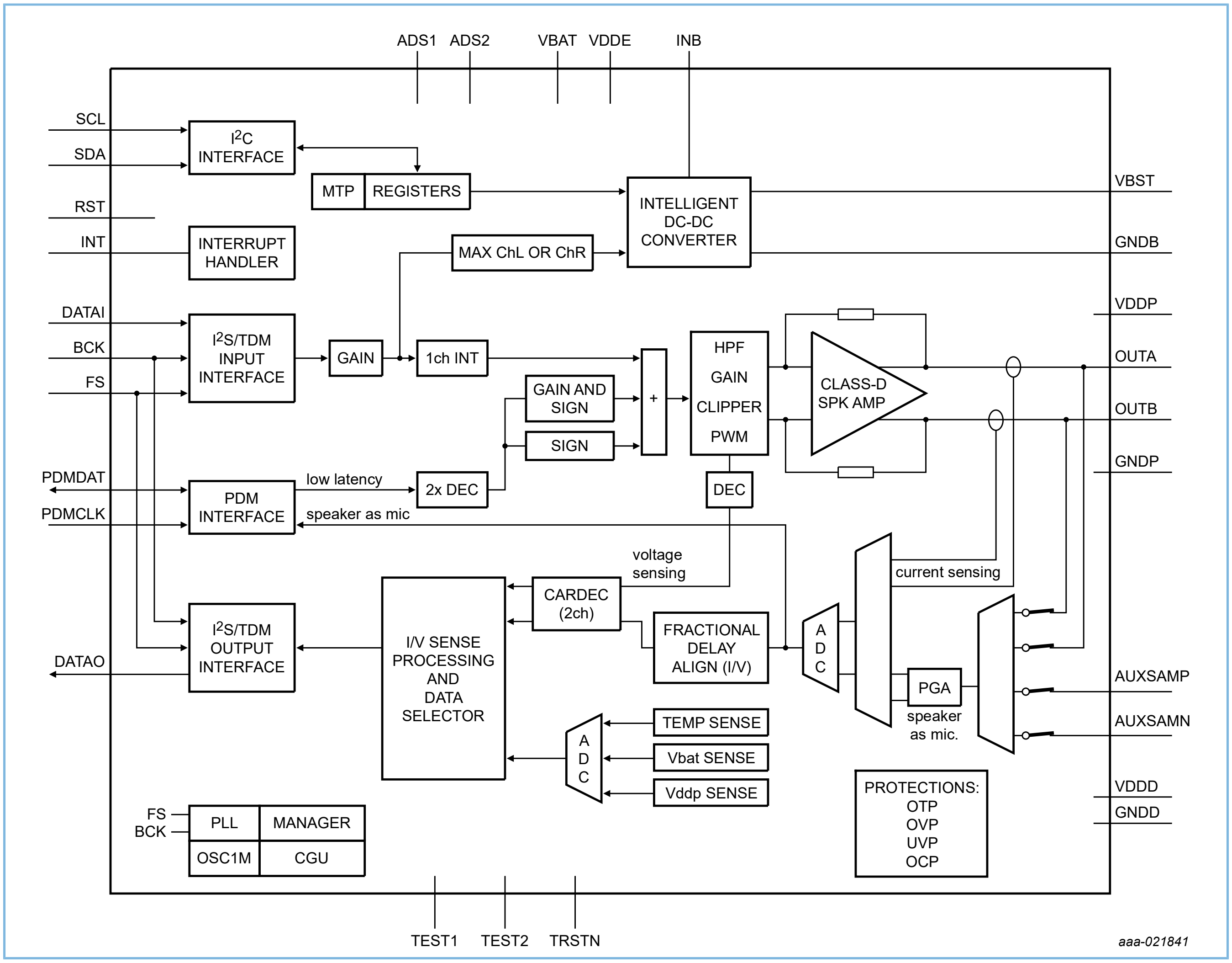


Figure 6-1: Block diagram

7 Pinning information

7.1 Pinning

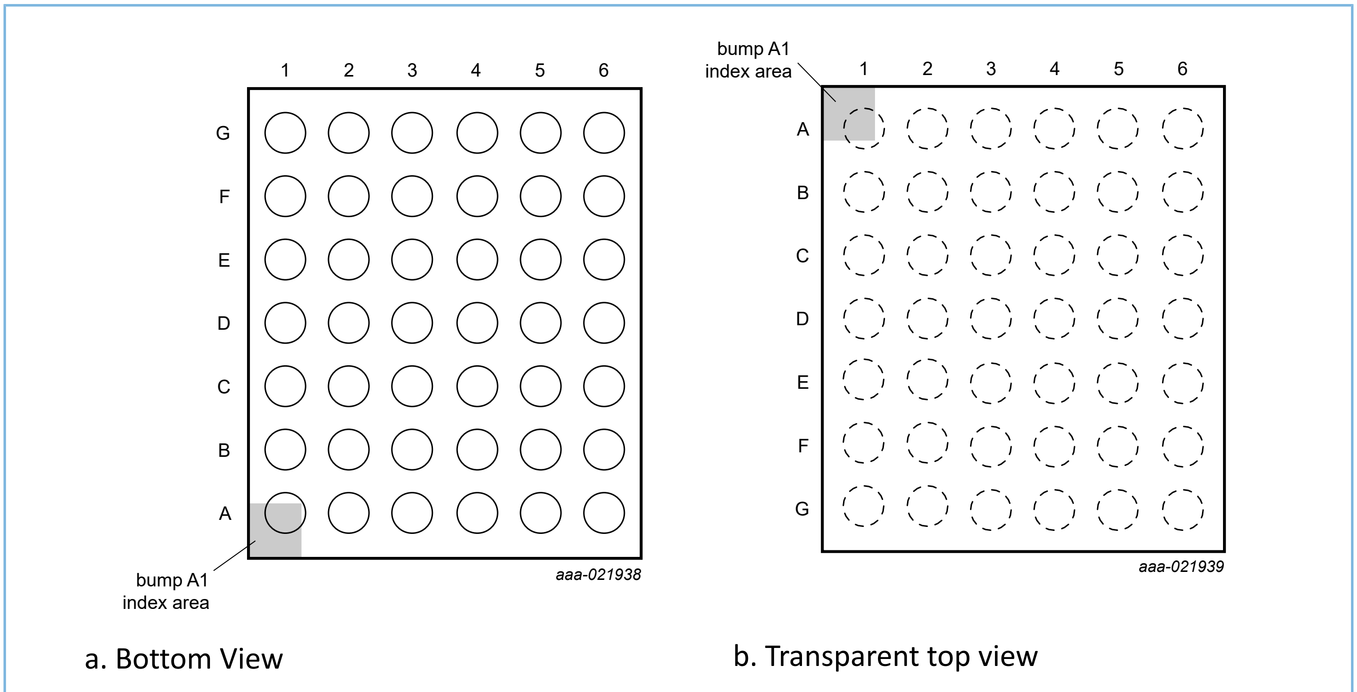


Figure 7-1: Bump configuration

	1	2	3	4	5	6
A	FS	DATAI	DATAO	GNDD	OUTB	VDDP
B	BCK	INT	RST	GNDP	GNDP	VDDP
C	PDMCLK	PDMDAT	TRSTN	GNDD	OUTA	VDDP
D	SCL	AUXSAMP	TEST2	GNDD	OUTA	VBST
E	SDA	AUXSAMN	TEST1	GNDB	INB	VBST
F	VDDD	ADS1	GNDD	GNDB	INB	VBST
G	VDDE	ADS2	VBAT	GNDB	INB	VBST

aaa-021936

Transparent top view

Figure 7-2: Bump mapping

7.2 Pin description

Table 7-1: Pinning

Symbol	Pin	Type	Description
FS	A1	I	digital audio frame sync for TDM/I^2S interface
DATAI	A2	I	digital audio data input for TDM/I^2S interface
DATAO	A3	O	digital audio data output for TDM/I^2S interface
GNDD	A4	P	digital ground
OUTB	A5	O	inverting output
VDDP	A6	P	power supply voltage
BCK	B1	I	digital audio bit clock input for TDM/I^2S interface
INT	B2	O	digital interrupt output
RST	B3	I	digital reset input
GNDP	B4	P	power ground
GNDP	B5	P	power ground
VDDP	B6	P	power supply voltage
PDMCLK	C1	I	digital audio clock for PDM interface
PDMDAT	C2	I	digital audio data for PDM interface
TRSTN	C3	I	test reset signal (for JTAG); connect to PCB ground
GNDD	C4	P	digital ground
OUTA	C5	O	non-inverting output
VDDP	C6	P	power supply voltage
SCL	D1	I	digital I^2C-bus clock input
AUXSAMP	D2	I/O	auxiliary speaker-as-microphone non-inverting input
TEST2	D3	I/O	test signal input 2; for test purposes only, connect to PCB ground
GNDD	D4	P	digital ground
OUTA	D5	O	non-inverting output
VBST	D6	O	boosted supply voltage output
SDA	E1	I	digital I^2C-bus data input
AUXSAMN	E2	I/O	auxiliary speaker-as-microphone inverting input

Symbol	Pin	Type	Description
TEST1	E3	I/O	test signal input 1; for test purposes only, connect to PCB ground
GNDB	E4	P	boosted ground
INB	E5	P	DC-to-DC boost converter input
VBST	E6	O	boosted supply voltage output
VDDD	F1	P	digital supply voltage
ADS1	F2	I	digital address select input 1
GNDD	F3	P	digital ground
GNDB	F4	P	boosted ground
INB	F5	P	DC-to-DC boost converter input
VBST	F6	O	boosted supply voltage output
VDDE	G1	P	digital IO supply voltage
ADS2	G2	I	digital address select input 2
VBAT	G3	P	battery supply voltage
GNDB	G4	P	boosted ground
INB	G5	P	DC-to-DC boost converter input
VBST	G6	O	boosted supply voltage output

8 Functional description

The TFA9872 is a highly efficient Bridge Tied Load (BTL) class-D audio amplifier embedding Speaker-as-Microphone (SaM) support, as depicted in the block diagram of *Figure 6-1*.

The TFA9872 contains a TDM/I^2S input/output interface for communicating with the audio host. The maximum number of slots is 16 (at f_s = 48 kHz) and the minimum number is 2 (I^2S mode). The interface is compliant with all I^2S interface configurations and supports a wide range of TDM interface configurations. It also features an optional ultrasonic path to the speaker.

The TFA9872 features a slave-configurable IN or OUT PDM interface. This audio interface can be connected to the audio host to provide a low-latency path (for side tone mixing) to the speaker. The 1-bit PDM stream is decimated and applied to the TDM interface. The PDM stream can, optionally, be attenuated or amplified by the gain module. Soft mute control prevents pop and click noise occurring when this signal path is switched on or off. The PDM output also provides a SaM stream back to the host.

At low battery voltage levels, the gain is automatically reduced to limit battery current (when battery safeguard is enabled).

The digital audio stream is converted into two PWM signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage when the audio stream crosses two programmable voltage thresholds. It switches automatically to Follower mode (V_{BST} = V_{BAT}; no boost) when the audio output voltage is lower than the battery voltage.

The SaM feature is available in both PDM and I^2S modes. This function can be used to turn the speaker into a dynamic microphone, providing an output audio stream on the digital interfaces. Due to the nature of the speaker membrane, the microphone equivalent characteristics perform best in high Sound Pressure Level (SPL) environments. Consequently, this feature is targeted at specific use cases such as concert recording or calls affected by wind noise. It is not intended to replace a primary/standard microphone but rather to complement it in such use cases by providing a signal that is less sensitive to saturation.

For SaM, a dedicated PGA is used to amplify the weak signal coming from the main speaker or receiver speaker. The result is a microphone that can handle high SPL environments.

SaM can be enabled on the main speaker connected to OUTA/OUTB, when the amplifier is off. Alternatively, SaM can be enabled on auxiliary inputs AUXSAMP/AUXSAMN, with the receiver speaker connected as input.

9 Limiting values

Table 9-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x	on pin VBAT		-0.3	+6	V
		on pins VBST, VDDP, AUXSAMP, AUXSAMN		-0.3	+12	V
		on pin INB, OUTA, OUTB	[1]	-0.3	+12	V
		on pins VDDD, VDDE, TEST1, TEST2		-0.3	+2.5	V
T_j	junction temperature			-40	+150	°C
T_{stg}	storage temperature			-55	+150	°C
T_{amb}	ambient temperature			-40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)		-2	+2	kV
		according to Charge Device Model (CDM)		-500	+500	V

[1] Using a Goodix demo board with a 1 mm wire/PCB track length on pin INB, AC pulses up to 18 V and -9 V can be observed without causing any damage as these spikes only partly penetrate the device (which is protected by internal clamp circuits).

10 Thermal characteristics

Table 10-1: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	36	K/W

11 Characteristics

11.1 DC characteristics

Table 11-1: DC characteristics

All parameters guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.0 V; Adaptive Boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT} V_{BAT} must not be lower than V_{DDD} or V_{DDE} in application		2.7	-	5.5	V
I_{BAT}	battery supply current	Active state on pin V_{BAT}; Operating mode with load R_L = 6 Ω; DC-to-DC in Adaptive Boost mode; P_o = 380 mW, (average music power), V_{BAT} = 4.0 V, V_{DDP} = 8.5 V		-	122	-	mA
		Idle state on pin V_{BAT}; Operating mode with load R_L = 6 Ω and no output signal (idle); DC-to-DC converter in Adaptive Boost mode; V_{BAT} = 4.0 V, V_{DDP} = 8.5 V		-	1.8	-	mA
		Power-down state on pin VBAT; DC-to-DC in power down mode; T_j = 25 °C, no clock.		-	1	-	µA
V_{DDP}	power supply voltage	on pin VDDP		2.7	-	10	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDE		1.65	1.8	1.95	V
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V
I_{DDD}	digital supply current	Active state on pin VDDD; Operating mode with load R_L = 6 Ω; DC-to-DC in Adaptive		-	6.8	-	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Boost mode; P_o = 380 mW, (average music power); V_{BAT} = 4.0 V;V_{DDP} = 8.5 V					
		Idle state on pin V_{DDD}; Operating mode with load R_L = 6 Ω and no output signal (idle); DC-to-DC converter in Adaptive Boost mode; V_{BAT} = 4.0 V, V_{DDP} = 8.5 V		-	4.1	-	mA
		Power-down state on pin VDDD; DC-to-DC in power down mode; T_j = 25 °C, no clock.		-	10	-	µA
Pins FS, BCK, DATAI, ADS1, ADS2, SCL, SDA, PDMCLK, PDMDAT, RST, TRSTN							
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	V_{DDD}	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDD}$	V
C_i	input capacitance		[2]	-	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin		-	-	0.1	µA
Pins DATAO, INT, PDMDAT, push-pull output stages							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		-	-	V_{DDD} - 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins SDA, open drain outputs, external 10 kΩ resistor to V_{DDD}							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		-	-	V_{DDD} - 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins OUTA, OUTB							
R_{DSon}	drain-source on-state resistance	PMOS + NMOS transistors		-	510	-	mΩ
Protection							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	150	°C
$V_{uvp(VBAT)}$	undervoltage protection voltage on pin VBAT			2.3	-	2.5	V
$I_{O(ocp)}$	overcurrent protection output current			2	-	-	A
DC-to-DC converter							
V_{BST}	boosted supply voltage	DCVOS = 111; Boost mode		9.32	9.5	9.68	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

11.2 AC characteristics

Table 11-2: AC characteristics

All parameters guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.0 V; Adaptive Boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(AV)}$	average output power	Hands-free speaker, THD+N = 1 %					
		R_L = 8 Ω; f_s = 48 kHz, V_{BST} = 9.5 V, V_{BAT} = 4.0 V		3.6	5.1	-	W
		R_L = 6 Ω; f_s = 48 kHz, V_{BST} = 9.5 V, V_{BAT} = 4.0 V		-	5.9	-	W
		R_L = 4 Ω; f_s = 48 kHz, V_{BST} = 9.5 V, V_{BAT} = 4.0 V		-	6.0	-	W
		R_L = 8 Ω; f_s = 48 kHz, V_{BST} = 8.5 V, V_{BAT} = 3.6 V		3.6	4.0	-	W
		R_L = 6 Ω; f_s = 48 kHz, V_{BST} = 8.5 V, V_{BAT} = 3.6 V		-	5.1	-	W
		R_L = 4 Ω; f_s = 48 kHz, V_{BST} = 8.5 V, V_{BAT} = 3.6 V		-	5.2	-	W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Receiver speaker.THD+N = 1 %; V_{BST} = 9.5 V,					
		R_L = 32 Ω; Voice mode		-	0.2	-	W
		R_L = 32 Ω; Audio mode		-	1.2	-	W
Amplifier output pins (OUTA and OUTB)							
$\|V_{O(offset)}\|$	output offset voltage	absolute value after trimming; V_{DDP} = 3.4 V to 9.5 V, V_{BAT} = 3.4 V to 5 V		-	-	1.0	mV
Amplifier performances							
η_{po}	output power efficiency	on pin VBAT; Operating mode with load; R_L = 6 Ω; DC-to-DC in Adaptive Boost mode, P_o = 380 mW, (average music power), V_{BAT} = 4.0 V, V_{DDP} = 8.5 V	[2]	-	80	-	%
		on pin VBAT; input: 100 Hz sine wave, R_L = 8 Ω; DC-to-DC in Adaptive Boost mode, V_{BAT} = 4.0 V, V_{DDP} = 8.5 V,P_o = 700 mW	[2]	-	90	-	%
		on pin VBAT; input: 100 Hz sine wave, R_L = 8 Ω; DC-to-DC in Adaptive Boost mode, V_{BAT} = 4.0 V, V_{DDP} = 8.5 V,P_o = 4 W	[2]	-	84	-	%
THD+N	total harmonic distortion-plus-noise	V_{DDP} > 9 V, P_o = 2.0 W, R_L = 8 Ω	[2]	-	0.04	0.09	%
		V_{DDP} > 9 V, P_o = 2.0 W, R_L = 4 Ω	[2]	-	-	0.09	%
$V_{n(o)}$	output noise voltage	A-weighted; DATAI = 0 V; Low Noise mode (ISTLA = 1); f_s = 48 kHz; PLL locked on BCK (jitter <1 ns (p-p))	[2]	-	19	24	µV
		A-weighted; DATAI = 0 V; Low Noise mode (ISTLA = 1); f_s = 16 kHz	[2]	-	55	60	µV
S/N	signal-to-noise ratio	A-weighted, V_{BAT} = 3.4 V to 5 V, maximum signal at THD = 1 %	[2]	100	-	-	dB
PSRR	power supply rejection ratio	from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 217 Hz		-	80	-	dB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		square wave, V_{ripple} = 50 mV(p-p), V_{BAT} = 4.0 V					
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 20 Hz to 1 kHz sine wave, V_{ripple} = 200 mV (RMS), V_{BAT} = 3.4 V to 5.0 V; Low Power and Low Noise modes on		60	80	-	dB
		from V_{BAT}; f_{ripple} = 20 Hz to 1 kHz sine wave, V_{ripple} = 200 mV (RMS), V_{BAT} = 3.4 V to 5.0 V; DC-DC in follower OR booster; Low Power and Low Noise modes off		-	75	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 1 kHz to 20 kHz sine wave, V_{ripple} = 200 mV (RMS), V_{BAT} = 3.4 V to 5.0 V		-	70	-	dB
ΔG/Δf	gain variation with frequency	BW = 20 Hz to 15 kHz, V_{BAT} = 3.4 V to 5 V		-0.1	-	0.7	dB
V_{POP}	pop noise voltage	at mode transition and gain change.				2	mV
R_L	load resistance			4	8	32	Ω
C_L	load capacitance			-	-	200	pF
f_{sw}	switching frequency	directly coupled to the I^2S input frequency		256	-	384	kHz
G_v	voltage gain	I^2S/TDM to V_O; INPLEV = 0 (0 dB)		6	-	21	dB
Amplifier power-up, power-down and propagation delays							
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK, f_s = 48 kHz		-	2	-	ms
		PLL locked on FS, f_s = 48 kHz		-	5	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time	f_s = 48 kHz	[3]	-	1	-	ms
$t_{d(off)}$	turn-off delay time			-	32	-	µs
$t_{d(alarm)}$	alarm delay time			-	200	-	ms
t_{PD}	propagation delay	f_s = 16 kHz (I^2S/TDM)		-	1750	-	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		f_s = 48 kHz (I^2S/TDM)		-	600	-	µs
		f_s = 96/192 kHz (I^2S/TDM)		-	320	-	µs
		f_s = 48 kHz (PDM)		-	70	-	µs
Booster Inductance							
L_{bst}	boost inductance			0.7	1.0	2.2	µH
Current-sensing performance							
$L_{L(spk)}$	speaker load inductance			30	-	-	µH
S/N	signal-to-noise ratio	I_O = 1.1A (peak); A-weighted		62	65	-	dB
ΔI_{sense}	current sense mismatch	over frequency; 20 Hz to 4 kHz		-	-	3	%
		over temperature; f_i = 1 kHz; T_j = -20 °C to 85 °C		-	2	-	%
		over V_{DDP}; f_i = 1 kHz, V_{DDP} = 2.7 V to 9.5 V		-	1	-	%
THD+N	total harmonic distortion-plus-noise	f_i = 20 Hz to 20 kHz; V_i = -6 dBFS; TDMSPKG = 0110		-	-	0.75	%
B	bandwidth		[2]	0.02	-	20	kHz
Speaker-as-microphone performance; pins OUTA, OUTB							
GPGA	PGA gain	PGAGAIN = 30 dB (± 1.5 dB accuracy)		-	27.6	-	dB
		PGAGAIN = 24 dB (± 1.5 dB accuracy)		-	22.2	-	dB
		PGAGAIN = 18 dB (± 1.5 dB accuracy)		-	16.8	-	dB
		PGAGAIN = 16 dB (± 1.5 dB accuracy)		-	14.9	-	dB
$V_{i(max)}$	maximum input voltage	PGAGAIN = 18 dB; RMS value	[4]	-	10.5	-	mV
		PGAGAIN = 30 dB; RMS value	[4]	-	3.0	-	mV
$V_{n(i)(eq)}$	equivalent input noise voltage	A-weighted, PGAGAIN: 30 dB; TDM Output; RMS value		-	1.05	-	µV
		A-weighted, PGAGAIN: 16 dB; TDM Output; RMS value		-	2.35	-	µV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		A-weighted, PGAGAIN: 30 dB; PDM Output; RMS value		-	1.20	-	µV
		A-weighted, PGAGAIN: 16 dB; PDM Output; RMS value		-	1.35	-	µV
S/N	signal-to-noise ratio	A-weighted; PDM output; full scale input; PGAGAIN: 18 dB;		-	78.6	-	dB
		A-weighted; PPDM Output Full scale input, PGA gain setting GAIN_00		-	70.3	-	dB
		A-weighted; PTDM output; full scale input; PGAGAIN: 18 dB;		-	76.9	-	dB
		TDM output; full scale input; PGAGAIN: 30 dB		-	69.6	-	dB
THD+N	total harmonic distortion-plus-noise	f_i = 1 kHz, V_i = 0.5ΩmV (RMS), maximum PGA gain setting (30 dB), on pin OUTA/OUTB		-	0.3	-	%
		f_i = 1 kHz, V_i = 0. 5 mV (RMS), maximum PGA gain setting (30 dB), on pin AUXSAMN/AUXSAMP		-	0.45	-	%
PSRR	power supply rejection ratio	square wave on VDDD, f_{ripple} = 217 Hz, V_{ripple} = 50 mV (p-p), maximum PGA gain setting (**30 dB**)		-	70	-	dB
		sine wave on VDDD, f_{ripple} = 20 Hz to 1 kHz, V_{ripple} = 100 mV (RMS), maximum PGA gain setting (30 dB)		-	70	-	dB
		sine wave on VDDD, f_{ripple} = 1 kHz to 20 kHz, V_{ripple} = 100 mV (RMS), maximum PGA gain setting (30 dB)		-	60	-	dB
$V_{O(offset)}$	output offset voltage	% of Full Scale; PDM output only (offset is removed on TDM output)	[5]	-10	-	10	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[3] At power up, audio is output on OUTA/OUTB after $t_{d(on)amp}$ + $t_{d(on)PLL}$.
[4] Overload level at input; output is specified at 0 dBFS for TDM/PDM output max, or output limited at THD+N =1 % if reached before 0 dBFS; THD = 1 %.
[5] When using PDM output for Speaker-as-Microphone, PDM stream decimation shall be done in codec or AP running SAM software and it must include a DC offset remover.

11.3 I²S timing characteristics

Table 11-3: I²S bus interface characteristics; see *Figure 11-1*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.0 V, Adaptive Boost mode; L_{BST} = 1 μH[1];R_L = 8 Ω[1]; L_L = 44 μH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin FS, audio mode	[2]	16	-	48	kHz
		on pin FS, ultrasonic mode		96	-	192	kHz
f_{clk}	clock frequency	on pin BCK, audio mode	[2]	$32f_s$	-	$384f_s$	kHz
		on pin BCK, ultrasonic mode		-	-	$96f_s$	MHz
t_{su}	set-up time	FS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to FS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns
$t_{jit(p-p)}$	peak-to-peak jitter	PLL locked on BCK	[4]	-	1	-	ns
		PLL locked on FS	[5]	-	20	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] The I²S bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. Note that both the BCK and FS signals must be present for the clock to operate correctly.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[4] When the PLL is locked on BCK, amplifier output noise can deteriorate when clock jitter >1 ns.
[5] The system is less sensitive to jitter when the PLL is locked on FS.

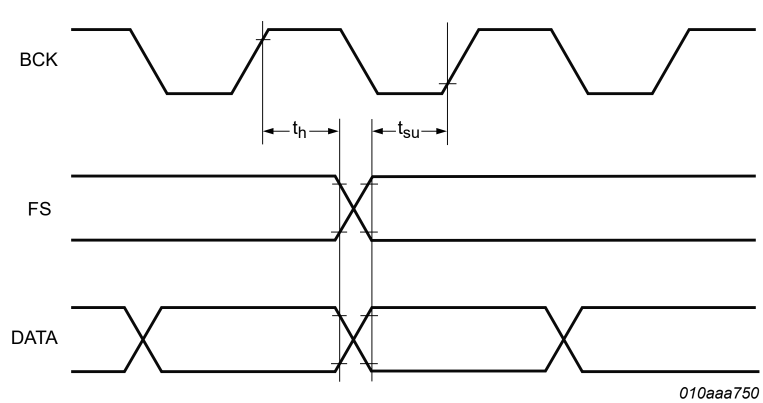


Figure 11-1: I²S timing

11.4 I^2C timing characteristics

Table 11-4: I^2C-bus interface characteristics; see *Figure 11-2*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.0 V, Adaptive Boost mode; L_{BST} = 1 µH[1];R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

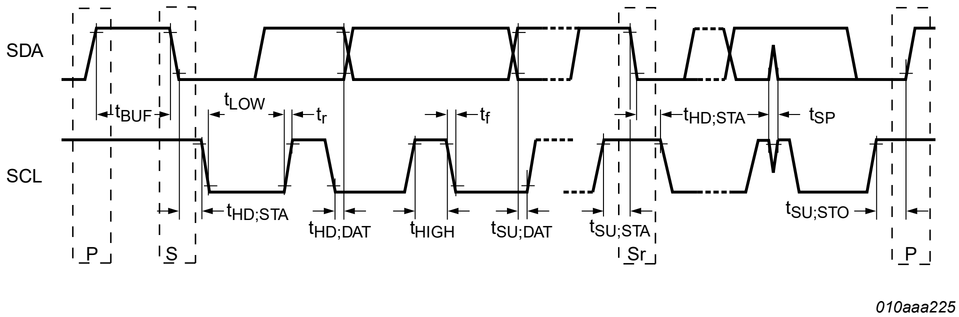


Figure 11-2: I^2C timing

11.5 PDM timing characteristics

Table 11-5: PDM interface characteristics; see *Figure 11-3*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.0 V, Adaptive Boost mode; L_{BST} = 1 μH[1];R_L = 8 Ω[1]; L_L = 44 μH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency		[2]	-	3.072	-	MHz
δ_{clk}	clock duty cycle			45	-	55	%
t_h	hold time	after clock HIGH		30	-	-	ns
		after clock LOW		30	-	-	ns
t_{su}	set-up time	after clock HIGH		30	-	-	ns
		after clock LOW		30	-	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] PDM Clock is 64xfs, with fs selected by AUDFS. Typical 3.072 Mhz is corresponding to f_s = 48 kHz.

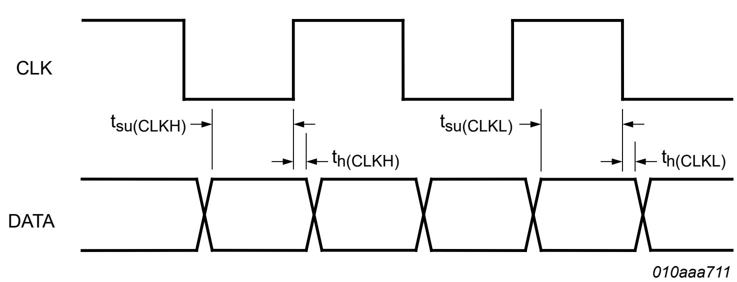


Figure 11-3: PDM timing

12 Application information

12.1 Application diagrams

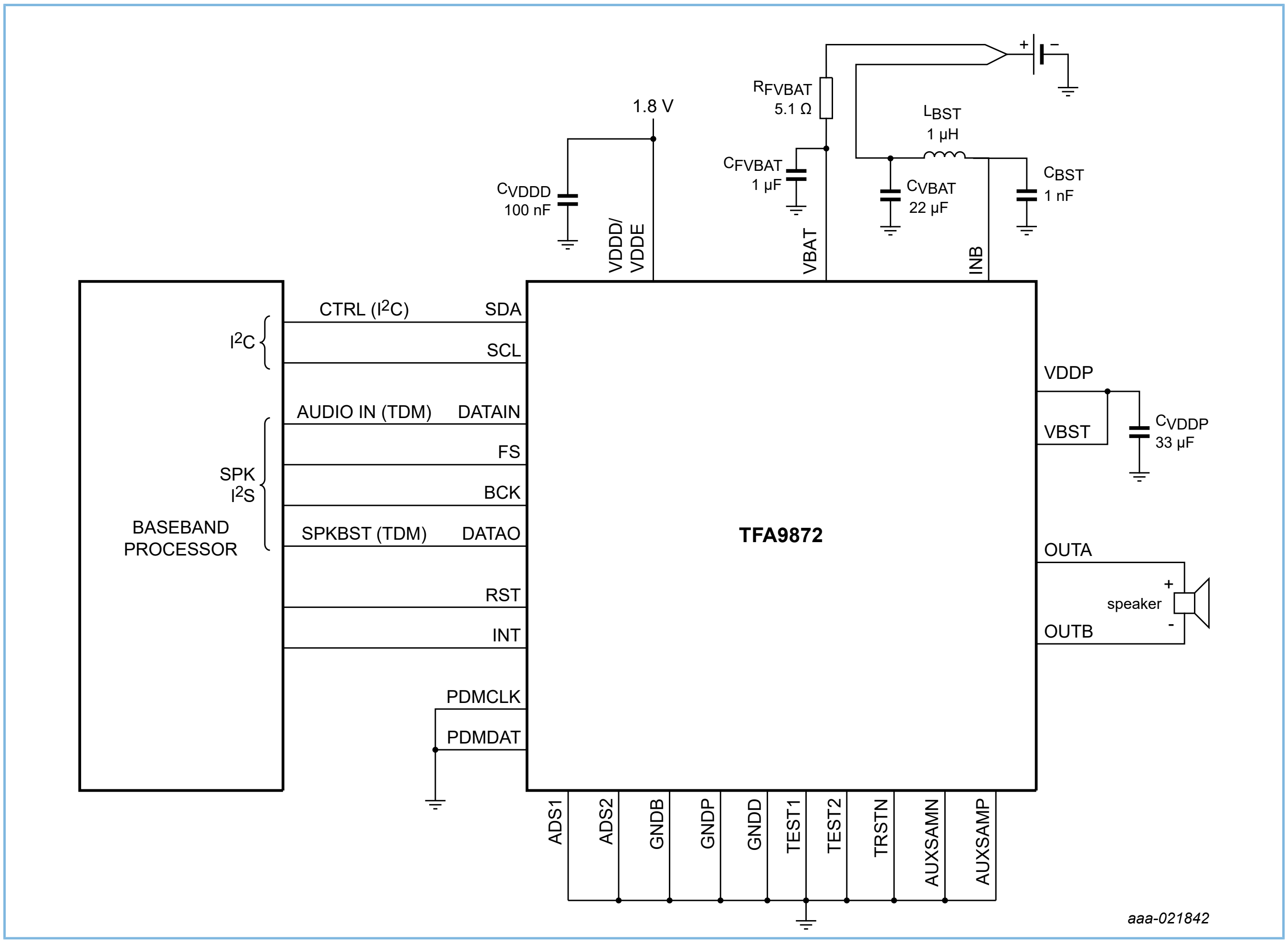


Figure 12-1: Typical mono application

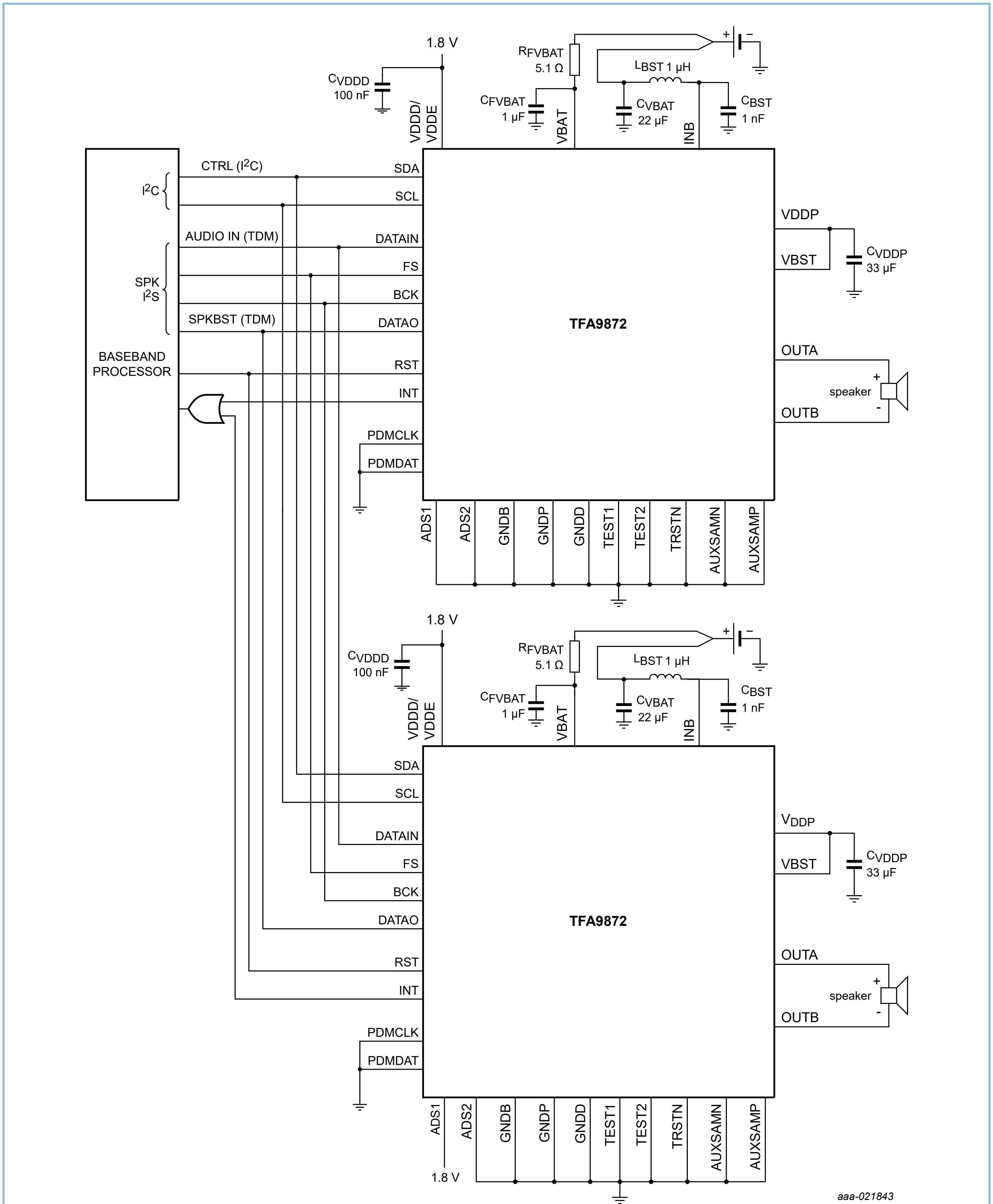


Figure 12-2: Typical stereo application (using separated coils)

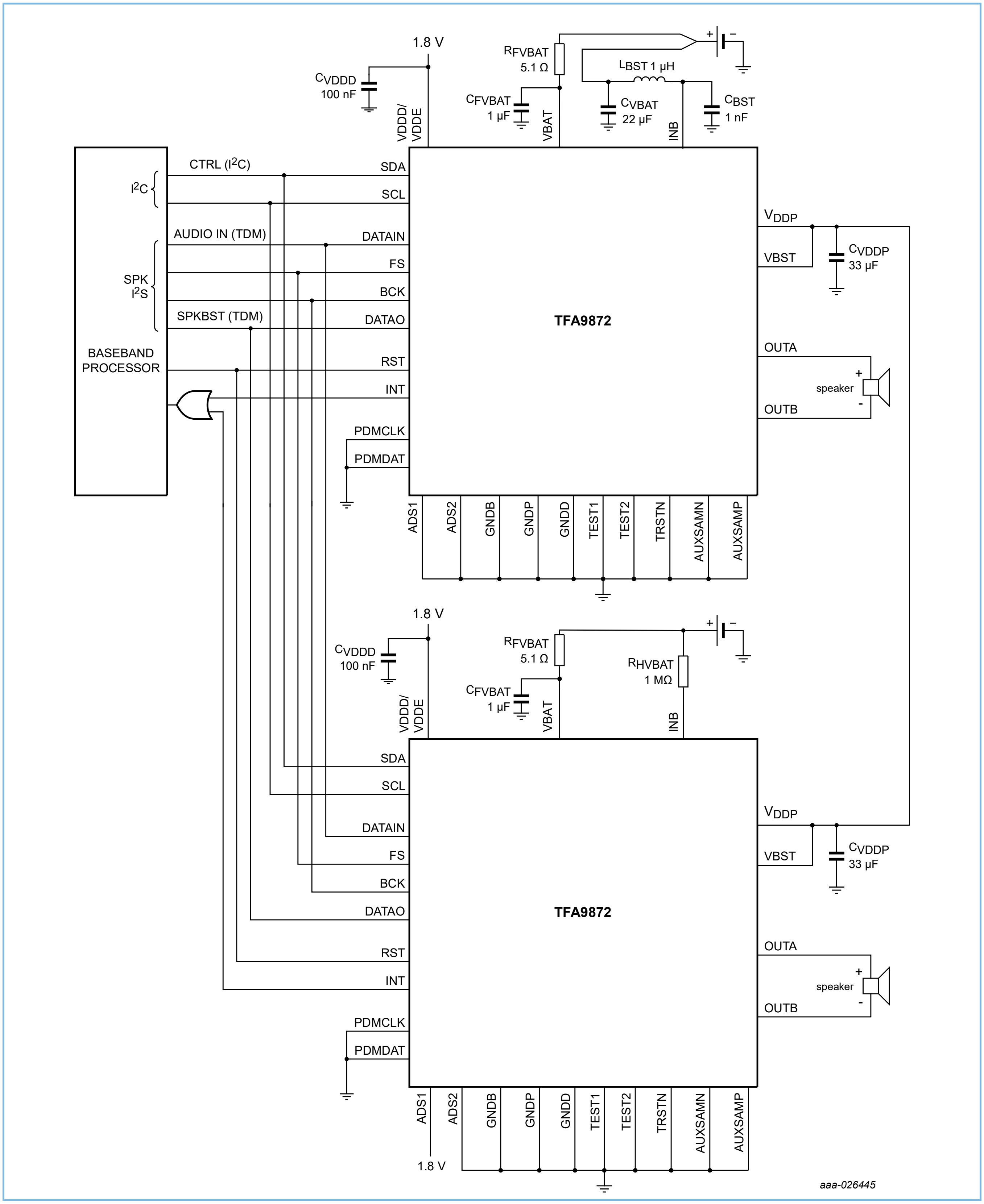
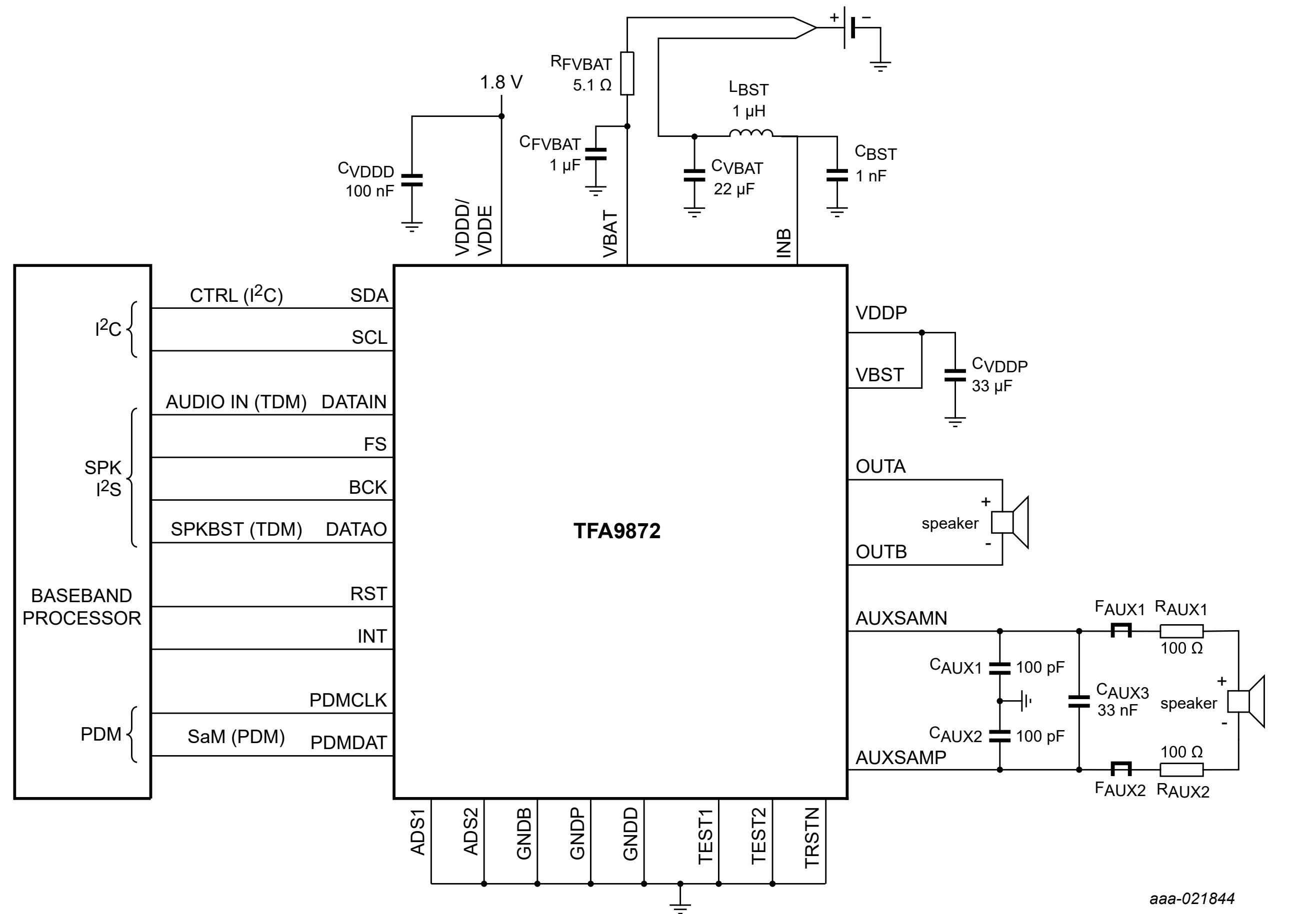


Figure 12-3: Typical stereo application (using a single coil)

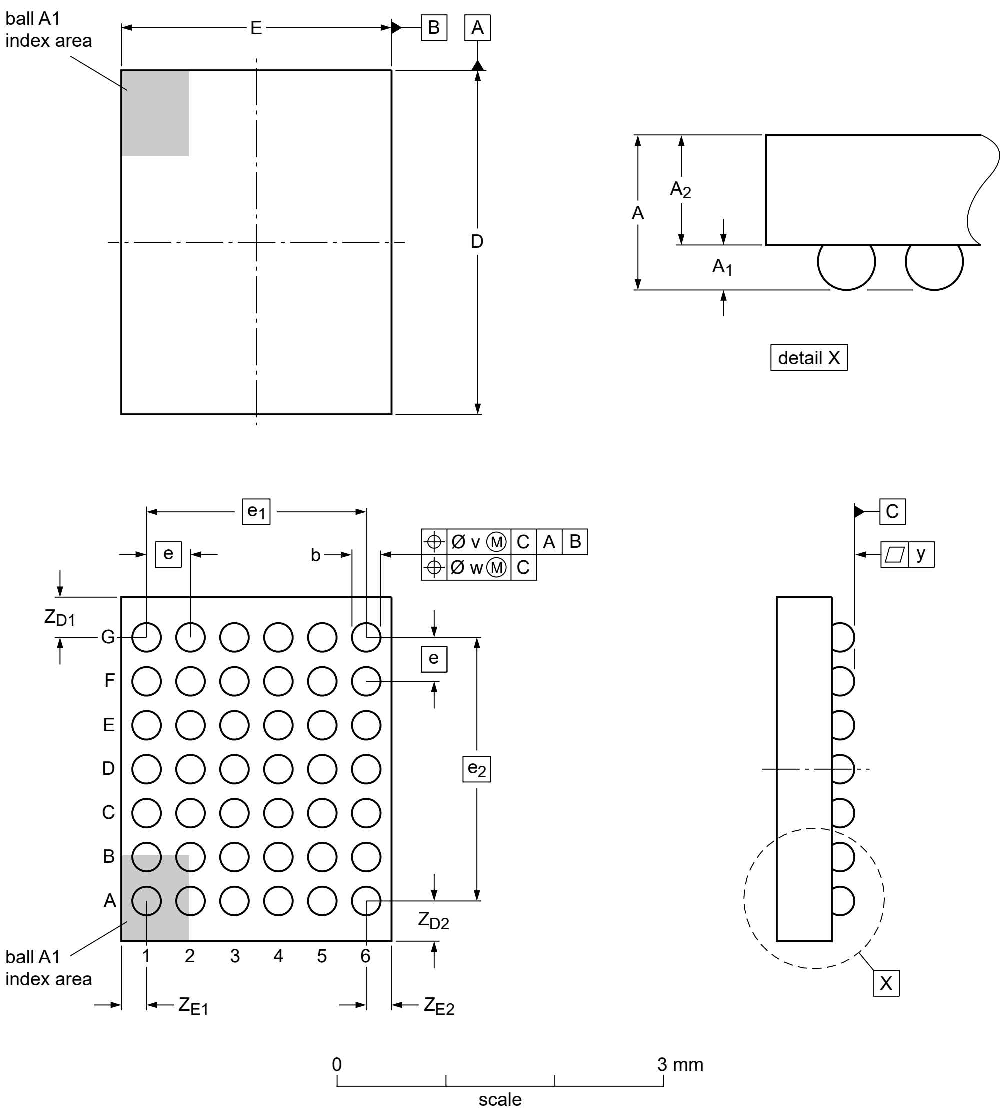


The configuration shown also supports speaker playback

Figure 12-4: Typical SaM application

13 Package outline

WLCSP42: wafer level chip-scale package; 42 bumps; 3.13 x 2.46 x 0.50 mm **SOT1459-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}	v	w	y
	max	0.54	0.23	0.325	0.29	3.16	2.49										
mm	nom	0.50	0.20	0.300	0.26	3.13	2.46	0.4	2.0	2.4	0.365	0.365	0.245	0.215	0.05	0.02	0.03
	min	0.46	0.17	0.275	0.23	3.10	2.43										

sot1459-2_po

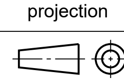
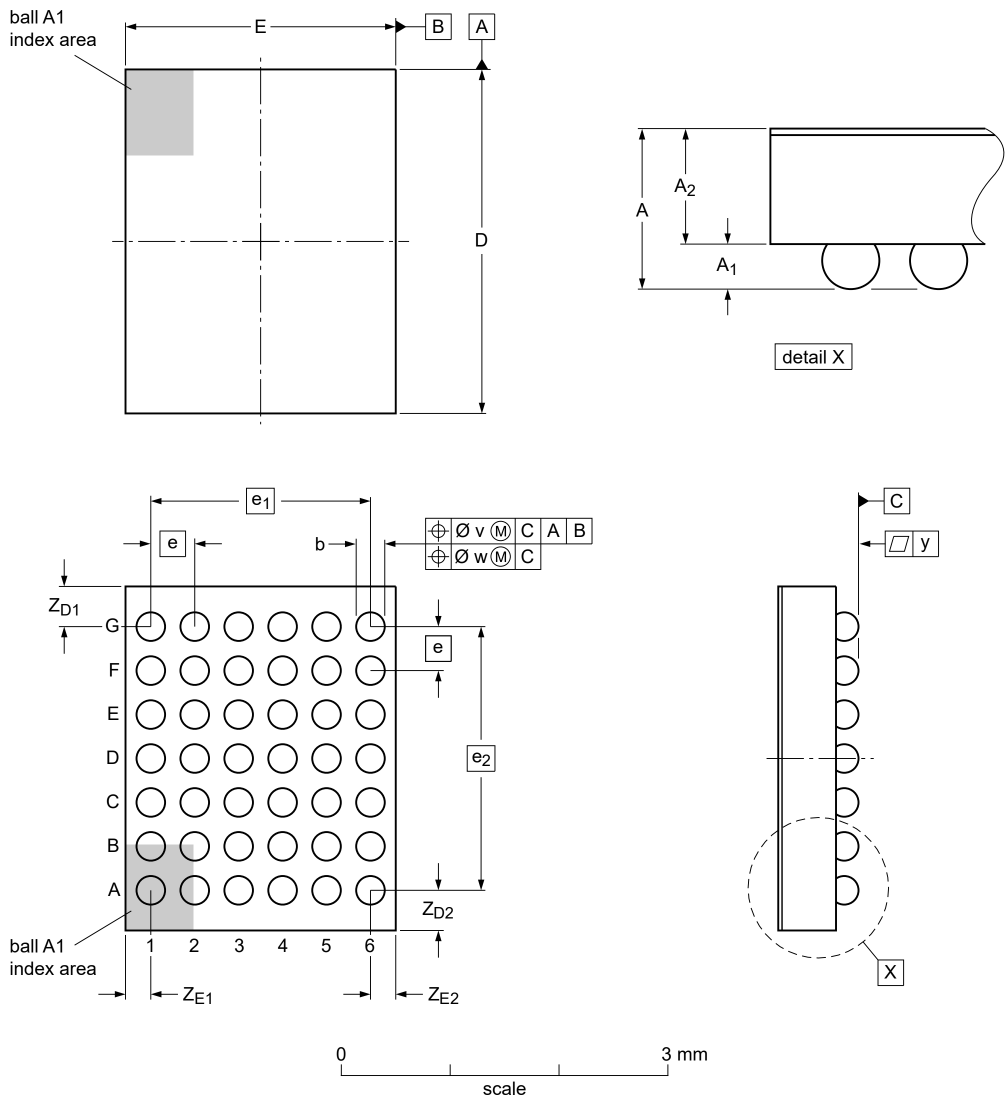
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1459-2		- - -				~~16-02-25~~ 16-03-01

Figure 13-1: Package outline TFA9872AUK/N1 (WLSCP42)

WLCSP42: wafer level chip-scale package; 42 bumps; 3.13 x 2.46 x 0.525 mm (backside coating included) **SOT1459-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}	v	w	y
mm	max	0.565				3.16	2.49										
	nom	0.525	0.20	0.33	0.26	3.13	2.46	0.4	2.0	2.4	0.365	0.365	0.245	0.215	0.05	0.02	0.03
	min	0.485				3.10	2.43										

Note: Backside coating 25 µm

sot1459-3_po

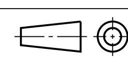
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1459-3		- - -				~~16-03-01~~ 16-05-09

Figure 13-2: Package outline TFA9872CUK/N1 (WLCSP42)

14 Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

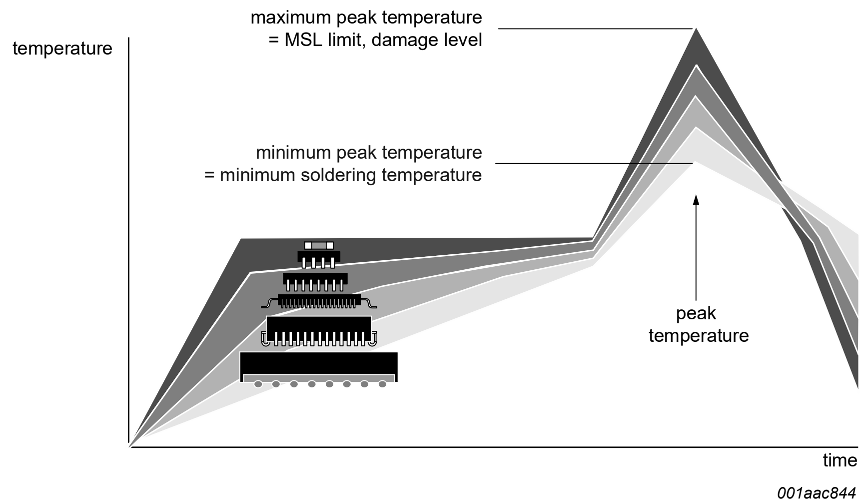
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 1) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with *Table 14-1*.

Table 14-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 1.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see *Figure 14-1*.



MSL: Moisture Sensitivity Level

Figure 14-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

  The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15 Legal and contact information

Trademarks and Permissions

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16 Revision history

Table 16-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9872_SDS v 3.0	20200121	Product short data sheet	-	TFA9872_SDS v.2
Modifications:	• Updated document format based on Goodix template			
TFA9872_SDS v.2	<tbd>	Product short data sheet	-	TFA9872_SDS v.1
Modifications:	• *Chapter 1*: text of 2nd last paragraph amended • *DC characteristics*: max. value of parameter V_{IH} on digital I/O pins changed • *AC characteristics*: measurement conditions changed for parameter $V_{n(o)}$; measurement added for parameter $t_{d(on)PLL}$; Table note 3 added • *I^2S timing characteristics*: added parameter tjit(p-p), Table note 4 and Table note 5			
TFA9872_SDS v.1	20170412	Product short data sheet	-	-