TFA9890A_SDS

9.5 V Boosted Audio System with Adaptive Sound Maximizer and Speaker Protection

Version: 3.1

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Contents

1 General description

The TFA9890A is a high efficiency class-D audio amplifier with a sophisticated speaker boost and protection algorithm. It can deliver 7.2 W peak output power into an 8 Ω speaker at a supply voltage of 3.6 V. The internal boost converter raises the supply voltage to 9.5 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9890A maximizes acoustic output while ensuring diaphragm displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures that the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker.

Unlike competing solutions, the adaptive sound maximizer algorithm uses feedback to accurately calculate both the temperature and the excursion, allowing the TFA9890A to adapt to changes in the acoustic environment.

Internal intelligent DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. This maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The TFA9890A also incorporates advanced battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which could cause a system undervoltage. The advanced processor minimizes the impact of a falling battery voltage on the audio quality by preventing distortion as the battery discharges.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The audio input interface is I^2S and the control settings are communicated via an I^2C-bus interface.

The device also provides the speaker with robust protection against ESD damage. In a typical application, no additional components are needed to withstand a 15 kV discharge on the speaker.

The TFA9890A is available in a 49-bump WLCSP (Wafer Level Chip-Size Package) with a 400 µm pitch.

2 Features and benefits

- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
  - Fully embedded software, no additional license fee or porting required
  - Total integrated solution that includes DSP, amplifier, DC-to-DC, sensing and more
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Speaker error detection (detects faulty speakers and enclosures)
- Output power: 3.6 W (RMS) into 8 Ω at 3.6 V supply voltage (THD = 1 %)
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Bandwidth extension option to increase low frequency response
- Compatible with standard Acoustic Echo Cancellers (AECs)
- High efficiency and low power dissipation
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Two I^2S inputs to support two audio sources
- I^2C-bus control interface (400 kHz)
- Dedicated speech mode with speech activity detector
- Speaker current and voltage monitoring (via the I^2S-bus) for Acoustic Echo Cancellation (AEC) at the host
- Fully short-circuit proof across the load and to the supply lines
- Sample frequencies from 8 kHz to 48 kHz supported
- 3 bit clock/word select ratios supported (32x, 48x, 64x)
- Option to route I^2S input direct to I^2S output to allow a second I^2S output slave device to be used in combination with the TFA9890A
- TDM interface supported (with limited functionality)
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- 15 kV system-level ESD protection without external components
- ‘Pop noise' free at all mode transitions

3 Applications

- Mobile phones
- Tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- MP3 players and portable media players
- Small audio systems

4 Quick reference data

Table 4-1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	2.7	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin V_{BAT} and in DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive Boost mode (no output signal, V_{BAT} = 3.6 V, V_{DDD} = 1.8 V)	-	4	-	mA
		Power-down mode	-	1	-	µA
I_{DDD}	digital supply current	on pin V_{DDD}; Operating modes; SpeakerBoost Protection activated	-	20	-	mA
		on pin V_{DDD}; Operating modes; CoolFlux DSP bypassed	-	6	-	mA
		on pin V_{DDD}; Power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V	-	10	-	µA
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; CLIP = 1				
		R_L = 8 Ω; f_s = 48 kHz	-	3.6	-	W
		R_L = 8 Ω; f_s = 32 kHz	-	3.7	-	W

5 Ordering information

Table 5-1: Ordering information

Type number	Package		
	Name	Description	Version
TFA9890AUK/N1	WLCSP49	wafer level chip-size package; 49 bumps; 3.37 x 2.97 mm	TFA9890A

6 Block diagram

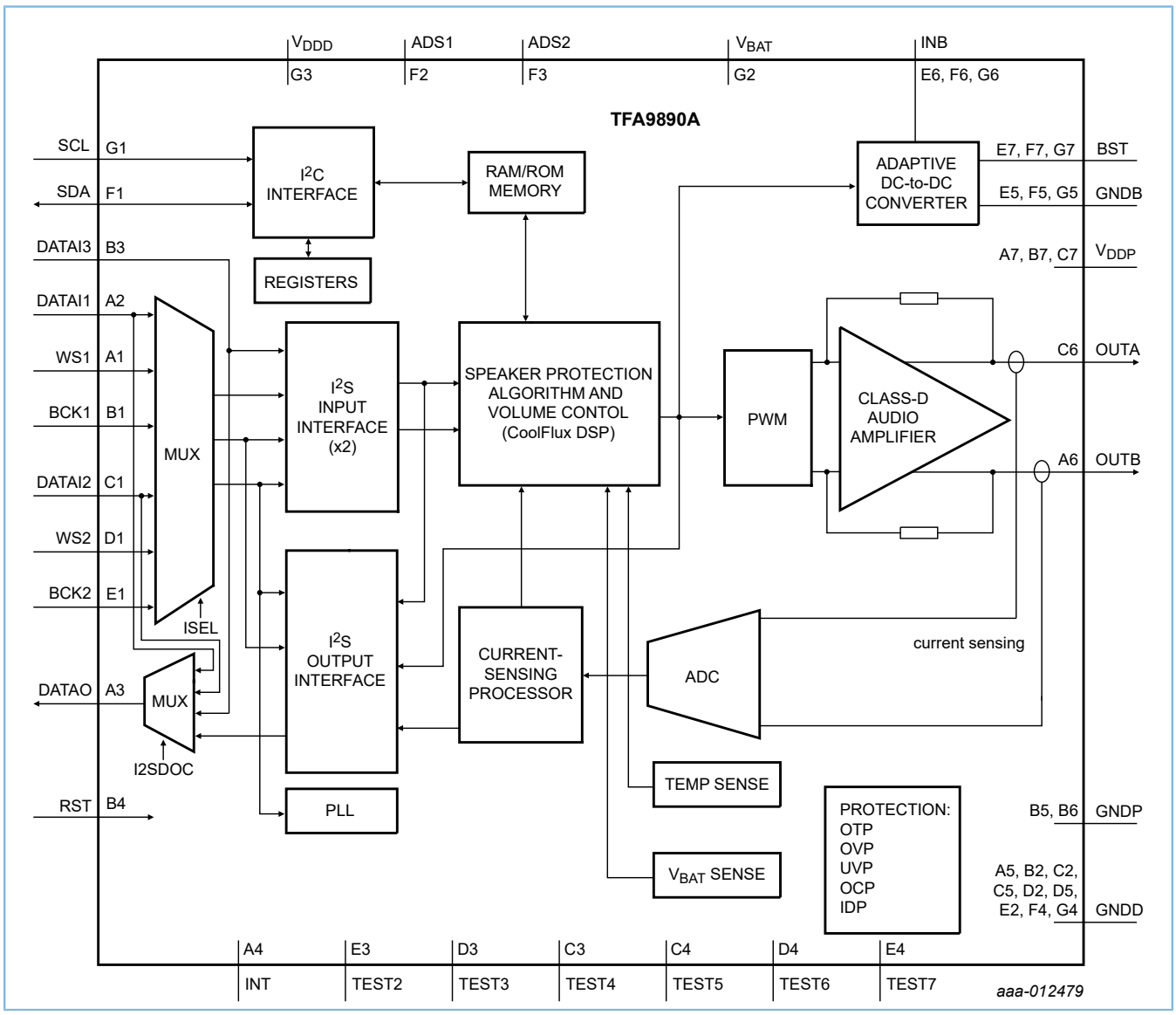
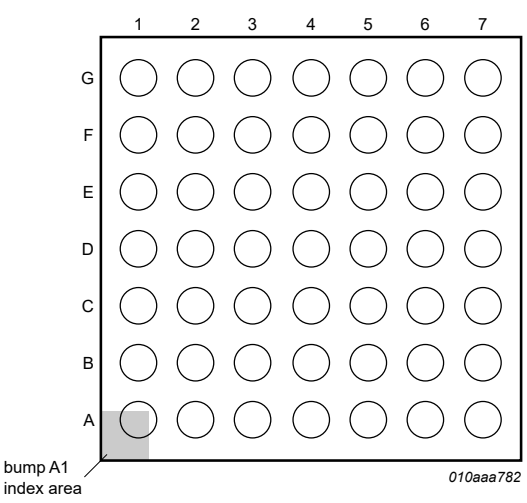


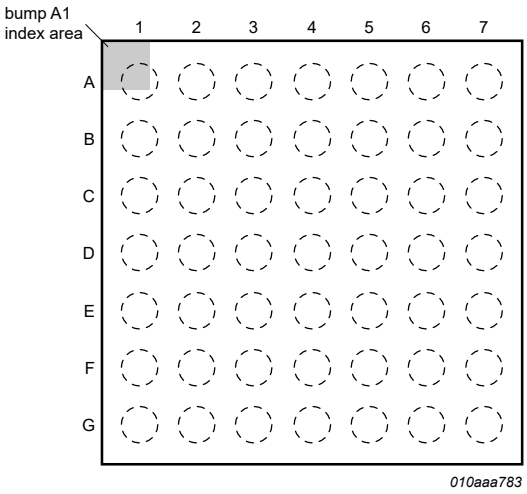
Figure 6-1: Block diagram

7 Pinning information

7.1 Pinning



a. Bottom View



b. Transparent top view

Figure 7-1: Bump configuration

	1	2	3	4	5	6	7
A	WS1	DATAI1	DATAO	INT	GNDD	OUTB	V_{DDP}
B	BCK1	GNDD	DATAI3	RST	GNDP	GNDP	V_{DDP}
C	DATAI2	GNDD	TEST4	TEST5	GNDD	OUTA	V_{DDP}
D	WS2	GNDD	TEST3	TEST6	GNDD	n.c.	n.c.
E	BCK2	GNDD	TEST2	TEST7	GNDB	INB	BST
F	SDA	ADS1	ADS2	GNDD	GNDB	INB	BST
G	SCL	V_{BAT}	V_{DDD}	GNDD	GNDB	INB	BST

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Transparent top view

Figure 7-2: Bump mapping

Table 7-1: Pinning

Symbol	Pin	Type		Description
WS1	A1	I		digital audio word select input 1

Symbol	Pin	Type		Description
DATAI1	A2	I		digital audio data input 1
DATAO	A3	O		digital audio data output
INT	A4	O		interrupt output
GNDD	A5	P		digital ground
OUTB	A6	O		inverting output
V_{DDP}	A7	P		power supply voltage
BCK1	B1	I		digital audio bit clock input 1
GNDD	B2	P		digital ground
DATAI3	B3	I		digital audio data input 3
RST	B4	I		reset input
GNDP	B5	P		power ground
GNDP	B6	P		power ground
V_{DDP}	B7	P		power supply voltage
DATAI2	C1	I		digital audio data input 2
GNDD	C2	P		digital ground
TEST4	C3	O		test signal input 4; for test purposes only, connect to PCB ground
TEST5	C4	O		test signal input 5; for test purposes only, connect to PCB ground
GNDD	C5	P		digital ground
OUTA	C6	O		non-inverting output
V_{DDP}	C7	P		power supply voltage
WS2	D1	I		digital audio word select input 2
GNDD	D2	P		digital ground
TEST3	D3	O		test signal input 3; for test purposes only, connect to PCB ground
TEST6	D4	O		test signal input 6; for test purposes only, connect to PCB ground
GNDD	D5	P		digital ground
n.c.	D6	-	[1]	not connected
n.c.	D7	-	[1]	not connected
BCK2	E1	I		digital audio bit clock input 2
GNDD	E2	P		digital ground

Symbol	Pin	Type		Description
TEST2	E3	O		test signal input 2; for test purposes only, connect to PCB ground
TEST7	E4	O		test signal input 7; for test purposes only, connect to PCB ground
GNDB	E5	P		boosted ground
INB	E6	P		DC-to-DC boost converter input
BST	E7	O		boosted supply voltage output
SDA	F1	I/O		I^2C-bus data input/output
ADS1	F2	I		address select input 1
ADS2	F3	I		address select input 2
GNDD	F4	P		digital ground
GNDB	F5	P		boosted ground
INB	F6	P		DC-to-DC boost converter input
BST	F7	O		boosted supply voltage output
SCL	G1	I		I^2C-bus clock input
V_{BAT}	G2	P		battery supply voltage sense input
V_{DDD}	G3	P		digital supply voltage
GNDD	G4	P		digital ground
GNDB	G5	P		boosted ground
INB	G6	P		DC-to-DC boost converter input
BST	G7	O		boosted supply voltage output

[1] Can be used to simplify routing to OUTA (see Figure 7-2).

8 Functional description

The TFA9890A is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost protection algorithm. Figure 6-1 is a block diagram of the TFA9890A.

It contains three I^2S input interfaces and one I^2S output interface. One of I^2S inputs DATAI1 and DATAI2 can be selected as the audio input stream. The third I^2S input, DATAI3, is provided to support stereo applications. A 'pass-through' option allows one of the I^2S input interfaces to be connected directly to the I^2S output. The pass-through option is provided to allow an I^2S output slave device (e.g. a CODEC), connected in parallel with the TFA9890A, to be routed directly to the audio host via the I^2S output.

The I^2S output signal on DATAO can be configured to transmit the DSP output signal, amplifier output current information, DATAI3 Left or Right signal information or amplifier gain information. The gain information can be used to facilitate communication between two devices in stereo applications.

A SpeakerBoost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of ±10 °C. Furthermore, advanced signal processing ensures that the audio quality is always acceptable.

The protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

Output sound pressure levels are boosted within given mechanical, thermal and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high-quality music in quiet environments.

The frequency response of the TFA9890A can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 8 are processed with 24-bit single precision.

At low battery voltage levels, the gain is automatically reduced to limit battery current. The output volume can be controlled by the SpeakerBoost protection algorithm or by the host application (external). In the latter case, the boost features of the SpeakerBoost protection algorithm must be disabled to avoid neutralizing external volume control.

The SpeakerBoost protection algorithm output is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the SpeakerBoost protection algorithm. It switches to Follower mode ($V_{BST} = V_{BAT}$; no boost) when the audio output voltage is lower than the battery voltage.

8.1 Amplifier operating modes

The TFA9890A supports five operating modes:

- **Power-down mode**, with low supply current
- **Operating mode**, in which the amplifier is fully operational
- **Mute mode**, in which the class-D output is switching but the audio input signal is suppressed

- **Off mode**, in which the device is biased, but the class-D output is floating
- **Fault mode**, when a protection mechanism (other than SpeakerBoost protection) has been activated

8.1.1 Power-down mode

Power consumption is at a minimum in Power-down mode. The TFA9890A switches to Power-down mode when:

- the reset input (pin RST) goes HIGH (all digital circuits, including the DSP and RAM memory, are reset)
- V_{DDD} is switched off (< 0.8 V), triggering a complete reset of the TFA9890A
- I^2C control bit I2CR is set to 1 (only the I^2C registers are reset, the DSP and RAM remain configured)
- I^2C control bit PWDN is set to 1 (the default setting, the TFA9890A is not reset when PWDN is set to 1)
- there is no valid clock signal on I^2S inputs BCK or WS (removing the I^2S clock signals does not cause the TFA9890A to be reset)

The I^2C-bus remains operational in Power-down mode with the PWM outputs floating.

8.1.2 Operating mode

Operating mode is selected by applying a valid clock signal (see Section 8.3) to the WS and BCK inputs.

In Operating mode, I^2S data input 1 or 2 (DATAI1/DATAI2) is used as the audio input. By default, the digital audio signal is processed in the CoolFlux DSP. The processed audio signal is converted into a 3-level modulated PWM signal that is fed to the output terminals.

By default, the CoolFlux DSP protects the speaker in Operating mode. When the DSP is bypassed, the I^2S audio input is fed directly to the amplifier with fixed gain. The peak output voltage is 8 V at -6 dBFS. If the input voltage is above this level, the output will clip and the DC-to-DC converter output may be distorted.

Without speaker protection, a high output voltage can damage the speaker. To avoid over-driving the speaker, it is advised only to bypass the DSP at reduced input levels and not to use the boost converter (see Section 8.4) when the CoolFlux DSP is bypassed.

Remark: In Operating mode, the TFA9890A expects the same frequency on WS as was selected via bits I2SSR in the I^2S control register (i.e. the input sample rate).

8.1.3 Mute mode

Soft muting is used to prevent audible pop noise. The transition from Operating mode to Mute mode and from Mute mode to Operating mode is implemented using an exponential function. The transition time is about 10 ms for a 48 kHz I^2S input signal, and it scales with the frequency of the input signal. The I^2S signal must be stable during the transition time.

Mute mode is implemented in the CoolFlux DSP core and is only available when CoolFlux is not bypassed.

8.1.4 Off mode

In off mode, the outputs of the class-D amplifier are floating and the device is fully biased. The transition to Off mode can be direct, or can be combined with a soft mute (providing the CoolFlux DSP is not bypassed; the I^2S clock and WS signals must be stable when soft mute is activated).

8.1.5 Fault mode

The TFA9890A switches to Fault mode when a protection mechanism is triggered. In Fault mode, the class-D outputs are floating.

8.2 I^2S interface and channel selection

I^2S input interfaces 1 and 2 (DATAI1 and DATAI2) are multiplexed internally to the I^2S interface block (see Figure 6-1). I^2C control bit ISEL is used to select the I^2S interface. The word select or bit clock signal of the selected I^2S input can be used as the reference signal for the I^2S input interface, the I^2S output interface and the Phased Locked Loop (PLL). For a sample rate of 8 kHz, it is advised to clock on BCK (bit clock) only (the I^2S sample rate is selected via bits I2SSR in the I^2S control register). To prevent pop and click noise, the TFA9890A should be in Off mode when the value of ISEL is changed.

Note that the PLL clock is used as a reference for the entire chip. Crosstalk to the I^2S clock must also be prevented in the application. Extreme clock jitter can affect the reliability of speaker measurements.

The I^2S output, DATAO, can be enabled (active) or disabled (floating). DATAO can also be connected directly to DATAI1, DATAI2 or DATAI3 by selecting pass-through mode.

8.3 Interface formats

The I^2S digital audio formats supported by the TFA9890A are listed in Table 8-1. The I^2S digital audio format for the input and output interface is selected via bits I2SF in the I^2S control register.

Table 8-1: I^2S-supported digital audio formats

Interface format (MSB first)	Supported data format		BCK frequency
I^2S (Philips) standard	up to 16-bit		$32f_s$
LSB-justified - 16 bits	16-bit		$32f_s$
I^2S (Philips) standard	up to 24-bit		$48f_s$
LSB-justified - 16 bits	16-bit		$48f_s$
LSB-justified - 18 bits	18-bit		$48f_s$
LSB-justified - 20 bits	20-bit		$48f_s$
LSB-justified - 24 bits	24-bit		$48f_s$
I^2S (Philips) standard	up to 24-bit		$64f_s$
MSB-justified	up to 24-bit	[1]	$64f_s$
LSB-justified - 16 bits	16-bit		$64f_s$
LSB-justified - 18 bits	18-bit		$64f_s$

Interface format (MSB first)	Supported data format		BCK frequency
LSB-justified - 20 bits	20-bit		$64f_s$
LSB-justified - 24 bits	24-bit		$64f_s$

[1] MSB-justified is not supported at $32f_s$ or $48f_s$. LSB justified can be used instead of MSB-justified at $32f_s$ since there is no difference in data format between MSB- and LSB-justified for 16-bit data.

The TFA9890A supports nine I^2S sample rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz and 48 kHz. The I^2S input sample rate is selected via bits I2SSR in the I^2S control register. To prevent pop and click noise, the TFA9890A should be in Power-down mode when the sample rate is changed. The BCK frequency (32, 48 or 64 times f_s) is set automatically.

Remark: The sample rate on the input interface should always be in line with the sample rate selected via I2SSR. The SpeakerBoost protection algorithm will not operate correctly if they are different.

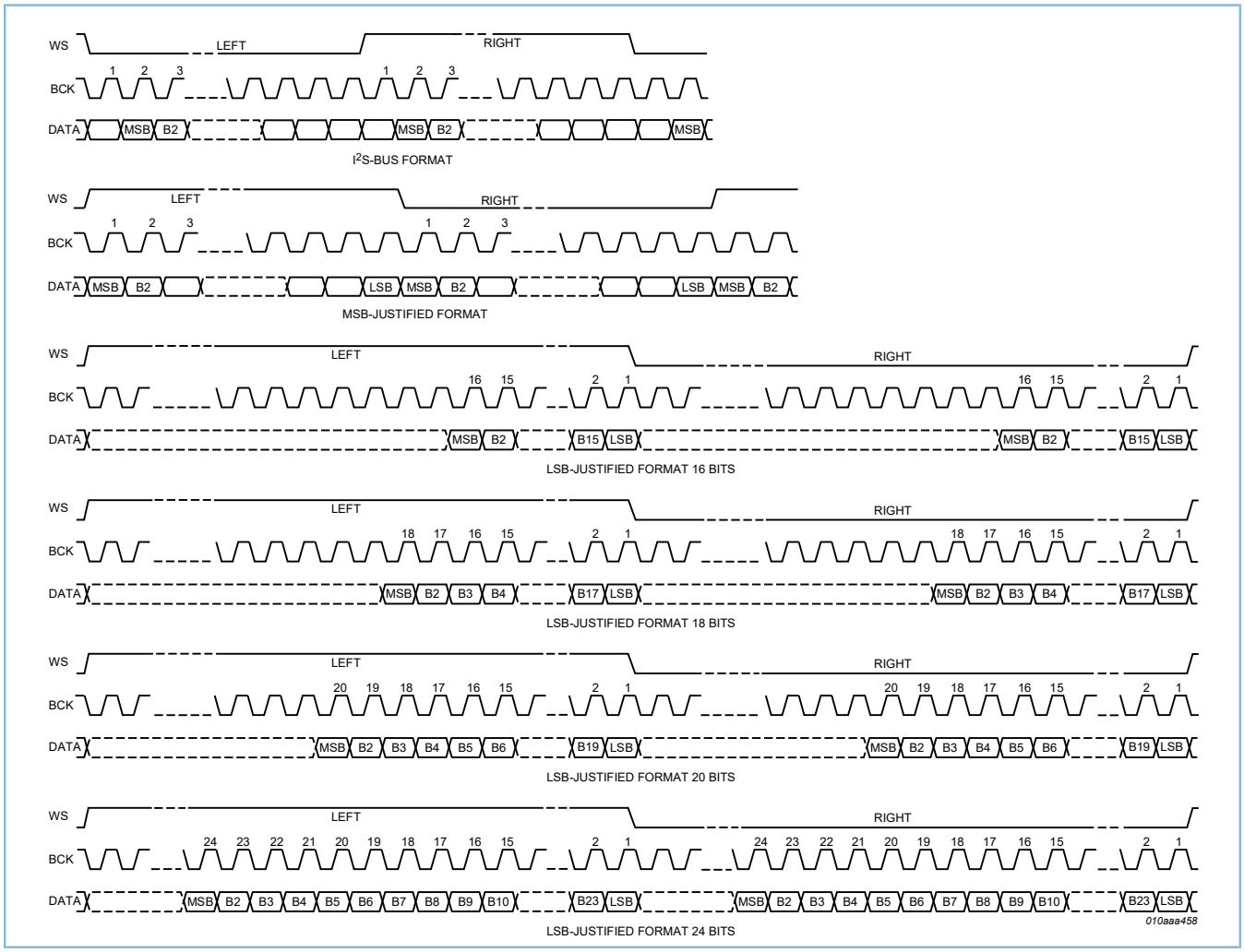


Figure 8-1: I^2S-supported digital audio data formats

8.4 DC-to-DC converter

The DC-to-DC converter in the TFA9890A operates independently of the amplifier. It features a feed-forward control function that lowers the ripple on the boosted output voltage.

Four converter modes are supported:

- **Disabled mode**, when the class-D amplifier is supplied externally (not via the internal DC-to-DC converter)
- **Follower mode**, when input INB is switched low-ohmic to V_{BST} (no boost; V_{BST} = battery voltage).
- **Boost mode**, when the battery voltage is boosted
- **Adaptive boost mode**, when the DC-to-DC converter boosts the battery voltage in line with the audio signal.

8.5 Battery supply safeguard

The TFA9890A employs a safeguard mechanism to protect the connected battery. This feature limits the TFA9890A current when the battery voltage falls below a programmable safeguard threshold (default is 3.53 V). The battery voltage is sensed via pin V_{BAT}.

8.6 Pulse width modulation controller

The PWM controller translates the digital input signal into a 3-level PWM output signal. The PWM switching frequency depends on the sample rate.

Table 8-2: PWM switching frequency of the class-D amplifier

Sample rate	f_{PWM}
f_s = 8, 16 or 32 kHz	256 kHz
f_s = 11.025, 22.05 or 44.1 kHz	352.8 kHz
f_s = 12, 24 or 48 kHz	384 kHz

8.7 Protection mechanisms

The following protection circuits are included in the TFA9890A:

- OverTemperature Protection (OTP)
- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- OverCurrent Protection (OCP)
- Invalid Data Protection (IDP)

The reaction of the device to fault conditions differs depending on the protection circuit involved.

8.8 Amplifier transfer function

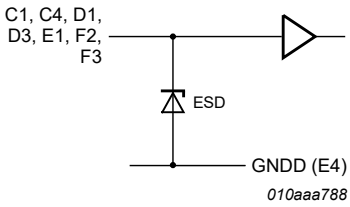
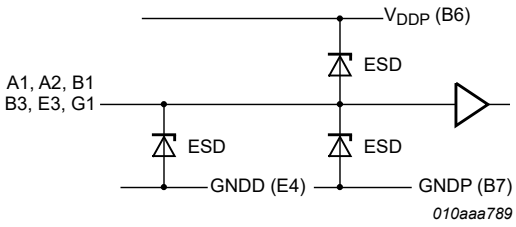
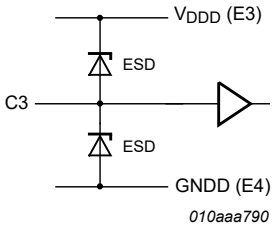
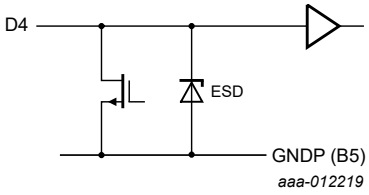
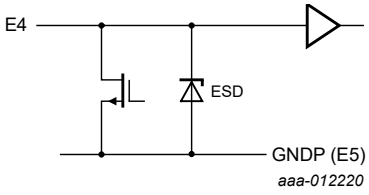
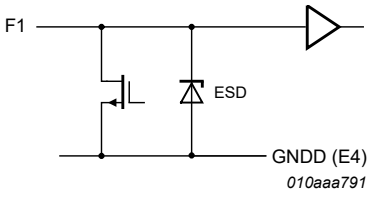
The transfer function from the CoolFlux DSP output (CFOUT) or directly from the I^2S input (CoolFlux DSP is bypassed) to the amplifier PWM outputs is:

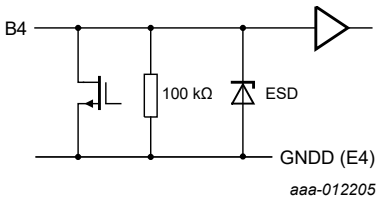
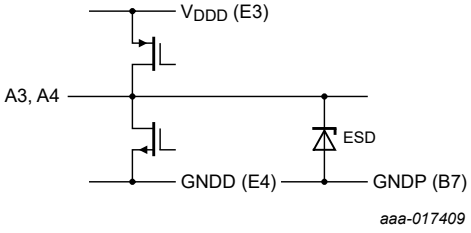
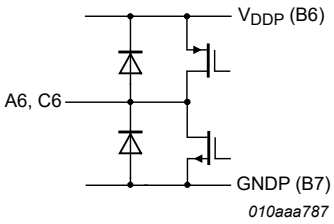
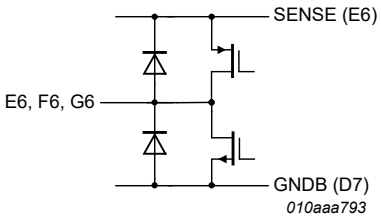
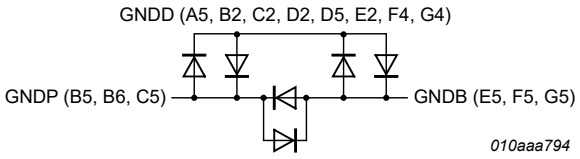
$$V_O = CF_{OUT} \times 16\text{V [V]} \quad (1)$$

The CF_{OUT} or I^2S signal is specified in a range from -1 to +1 (full scale dBFS).

9 Internal circuitry

Table 9-1: Internal circuitry

Pin	Symbol	Equivalent circuit
C1, C4, D1, D3, E1, F2, F3	DATAI2, TEST5, WS2, TEST3, BCK2, ADS1, ADS2	
A1, A2, B1, B3, E3, G1	WS1, DATAI1, BCK1, DATAI3, TEST2, SCL	
C3	TEST4	
D4	TEST6	
E4	TEST7	
F1	SDA	

Pin	Symbol	Equivalent circuit
B4	RST	
A3, A4	DATAO, INT	
A6, C6	OUTB, OUTA	
E6, F6, G6	INB	
A5, B2, B5, B6, C2, C5, D2, D5, E2, E5, F4, F5, G4, G5	GNDP, GNDB, GNDD	

10 I²C-bus interface and register settings

The TFA9890A supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control the TFA9890A and to transmit and receive data. The TFA9890A can only operate in I²C slave mode, as a slave receiver or as a slave transmitter.

10.1 TFA9890A addressing

The TFA9890A is accessed via an 8-bit code (see Table 10-1). Bits 1 to 7 contain the device address. Bit 0 (R/$\overline{W}$) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address, as detailed in Table 10-1. The generic address is independent of pins ADS1 and ADS2.

Table 10-1: Address selection via pins ADS1 and ADS2

ADS2 pin voltage (V)	ADS1 pin voltage (V)	Address	Function
0	0	01101000	for write mode
		01101001	for read mode
0	V_{DDD}	01101010	for write mode
		01101011	for read mode
V_{DDD}	0	01101100	for write mode
		01101101	for read mode
V_{DDD}	V_{DDD}	01101110	for write mode
		01101111	for read mode
don’t care	don’t care	00011100 (generic address)	for write mode
don’t care	don’t care	00011101 (generic address)	for read mode

11 Limiting values

Table 11-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	-0.3	+5.5	V
V_x	voltage on pin x	pin BST	-0.3	+12	V
		pins SDA and SCL	-0.3	+3.6	V
		pins DATAI1, WS1, BCK1, DATAI2, WS2, BCK2, RST and test pins	-0.3	+5.5	V
V_{DDP}	power supply voltage	on pin V_{DDP}	-0.3	+12	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	-0.3	+1.95	V
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	-2	+2	kV
		according to Charge Device Model (CDM)	-500	+500	V

12 Thermal characteristics

Table 12-1: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board positioned vertically in free air; dimensions: 30 × 19 × 1.6 mm; natural convection; copper coverage on each layer > 95 %; copper thickness outer/inner layer 35 µm	43	-	K/W

13 Characteristics

13.1 DC characteristics

Table 13-1: DC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1];L_L = 40 µH[1];f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}		2.7	-	5.5	V
V_{INB}	voltage on pin INB	boost converter input		2.7	-	5.5	V
I_{BAT}	battery supply current	on pin V_{BAT}		-	4	6	mA
I_{INB}	current on pin INB	no output signal		-	1	5	µA
		maximum output signal	[2]	-	-		mA
V_{DDP}	power supply voltage	on pin V_{DDP}		3	-	9.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		1.65	1.8	1.95	V
I_{DDD}	digital supply current	on pin V_{DDD}; Operating modes; SpeakerBoost Protection activated		-	20	-	mA
		on pin V_{DDD}; Operating modes; CoolFlux DSP bypassed		-	6	-	mA
		on pin V_{DDD}; Power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V		-	10	50	µA
Pins BCK1, WS1, DATA1, BCK2, WS2, DATAI2, DATAI3, ADS1, ADS2, SCL, SDA, RST							
V_{IH}	HIGH-level input voltage			0.7V_{DDD}	-	3.6	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DDD}	V
C_{in}	input capacitance		[3]	-	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin		-	-	0.1	µA
Pins DATAO, INT, push-pull output stages							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		-	-	V_{DDD} - 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins SDA, open-drain outputs, external 10 kΩ resistor to V_{DDD}							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		-	-	V_{DDD} - 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins OUTA, OUTB							
R_{DSon}	drain-source on-state resistance	V_{DDP} = 9.5 V		-	200	-	mΩ
Protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	150	°C
$V_{ovp(VBAT)}$	overvoltage protection voltage on pin VBAT			5.5	-	6.0	V
$V_{uvp(VBAT)}$	undervoltage protection voltage on pin VBAT			2.3	-	2.5	V
$I_{O(ocp)}$	overcurrent protection output current			2	-	-	A
DC-to-DC converter							
V_{BST}	voltage on pin BST	DCVO = 111; Boost mode		9.4	9.5	9.6	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] Maximum value determined by the I^2C setting.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

13.2 AC characteristics

Table 13-2: AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH [1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; CLIP = 1					
		R_L = 8 Ω; f_s = 48 kHz		-	3.6	-	W
		R_L = 8 Ω; f_s = 32 kHz		-	3.7	-	W
		THD+N = 10 %; CLIP = 1					
		R_L = 8 Ω; f_s = 48 kHz		-	4.5	-	W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		R_L = 8 Ω; f_s = 32 kHz		-	4.6	-	W
Amplifier output; pins OUTA and OUTB							
$\|V_{O(offset)}\|$	output offset voltage	absolute value		-	-	6	mV
Amplifier performance							
η_{po}	output power efficiency	$P_{o(RMS)}$ = 2.5 W; including DC-to-DC converter; 100 Hz audio signal	[2]	-	72	-	%
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)}$ = 100 mW; R_L = 8 Ω; L_L = 44 µH	[1]	-	0.03	0.1	%
$V_{n(o)}$	output noise voltage	A-weighted; DATAI1 = DATAI2 = 0 V					
		CoolFlux DSP bypassed		-	50	-	µV
		CoolFlux DSP enabled	[2]	-	66	-	µV
S/N	signal-to-noise ratio	V_O = 4.5 V (peak); A-weighted					
		CoolFlux DSP bypassed		-	100	-	dB
		CoolFlux DSP enabled; CLIP = 1	[2]	-	97	-	dB
PSRR	power supply rejection ratio	V_{ripple} = 200 mV (RMS); f_{ripple} = 217 Hz		-	75	-	dB
f_{sw}	switching frequency	directly coupled to the I^2S input frequency		256	-	384	kHz
V_o	output voltage	CoolFlux DSP bypassed; -1 to +1 (full scale dBFS) digital input		-	16	-	V
Amplifier power-up, power-down and propagation delays							
$t_{d(on)}$	turn-on delay time	PLL locked on BCK (IPLL = 0)					
		f_s = 8 kHz to 48 kHz		-	-	2	ms
		PLL locked on WS (IPLL = 1)					
		f_s = 8 kHz		-	-	27	ms
		f_s = 48 kHz		-	-	6	ms
$t_{d(off)}$	turn-off delay time			-	-	10	µs
$t_{d(mute\_off)}$	mute off delay time			-	1	-	ms
$t_{d(soft\_mute)}$	soft mute delay time		[3]	-	12	-	ms
$t_{d(pilot\_off)}$	pilot off delay time	after a soft mute; f_s = 48 kHz	[3]	-	11	21	ms

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		after a soft mute; f_s = 32 kHz		-	16	32	ms
t_{PD}	propagation delay	CoolFlux bypassed					
		f_s = 8 kHz		-	-	3.2	ms
		f_s = 48 kHz		-	-	600	µs
		SpeakerBoost protection mode, $t_{LookAhead}$ = 2 ms					
		f_s = 8 kHz		-	-	14	ms
		f_s = 48 kHz		-	-	4	ms
Current-sensing performance							
S/N	signal-to-noise ratio	I_O = 1.2 A (peak); A-weighted		-	75	-	dB
$I_{sense(acc)}$	sense current accuracy	I_O = 0.5 A (peak)		-3	-	+3	%
B	bandwidth		[3]	-	8	-	kHz
L_L	load inductance			20	-	-	µH

[1] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[3] The soft mute delay is the delay of the cosine role off of the audio. The pilot tone is removed at the zero crossing after a soft mute, with a delay of $t_{d(pilot\_off)}$. This takes a maximum of 21 ms (average 11 ms) at an input sample rate of 12 kHz, 24 kHz or 48 kHz. At an input sample rate of 8 kHz, 16 kHz or 32 kHz, the delay is 32 ms (max). So the worst case mute delay is 12 + 21 = 33 or 12 + 32 = 44 ms, depending on the sample frequency.

13.3 I^2S timing characteristics

Table 13-3: I^2S bus interface characteristics; see Figure 13-1

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω [1] ; L_L = 40 µH [1] ; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin WS	[2]	8	-	48	kHz
f_{clk}	clock frequency	on pin BCK	[2]	$32f_s$	-	$64f_s$	Hz
t_{su}	set-up time	WS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to WS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] The I^2S bit clock input (BCK) is used as a clock input for the DSP, as well as for the amplifier and the DC-to-DC converter. Both the BCK and WS signals must be present for the clock to operate correctly.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

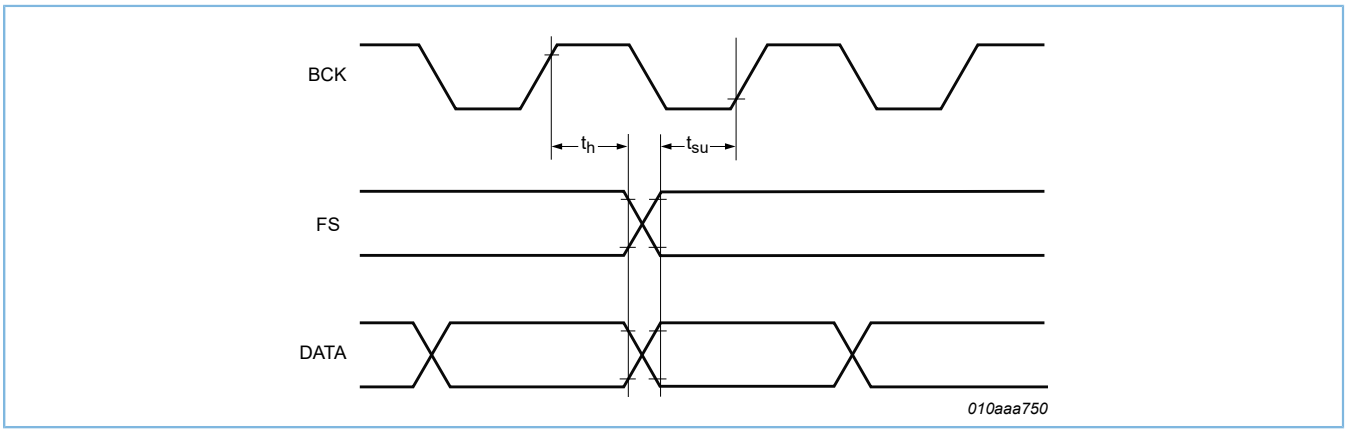


Figure 13-1: I^2S timing

13.4 I^2C timing characteristics

Table 13-4: I^2C-bus interface characteristics; see Figure 13-2

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1] ; L_L = 40 µH[1] ; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

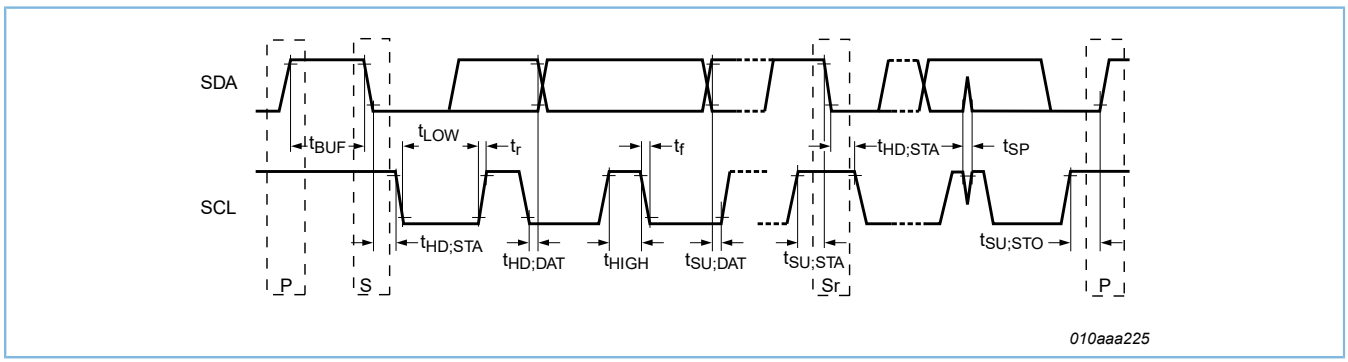


Figure 13-2: I²C timing

14 Application information

14.1 External components

Figure 14-1 shows the minimum number of external components needed in an application. The DC-to-DC converter needs a battery supply voltage capacitor (C_{VBAT}), an output capacitor (C_{VDDP}) and an inductor (L_{BST}) to work properly. The nominal values of these components are 10 nF, 20 µF and 1 µH, respectively. A 100 nF decoupling capacitor (C_{VDDD}) must be connected close to the V_{DDD} pin. The total capacitance at this supply line should be at least 1 µF.

14.1.1 DC-to-DC converter output capacitor

A ceramic capacitor is required at the output of the DC-to-DC converter (C_{VDDP}).

Capacitors constructed using X5R (-55 °C to +85 °C) or X7R (-55 °C to +125 °C) dielectric materials are preferred because they are compact, feature low ESR and are sufficiently stable over a wide temperature range. The capacitance value decreases over the DC biasing voltage range (30 % to 70 % decrease). Consequently, the nominal value of the capacitor should be close to twice the minimum value specified.

Remark: The DC-to-DC converter capacitor connected to BST is critical for stability. The recommended effective value (the capacitance value at the maximum boost voltage) of C_{VDDP} depends on the coil inductance, and is given in Table 14-1. The position of the capacitor and the layout of the board are also critical. It is recommended to connect C_{VDDP} as close as possible to the BST and GNDD pins without vias in the PCB tracks.

In many applications, it is desirable to limit the height of components as much as possible. This can be achieved for C_{VDDP} by connecting two smaller capacitors in parallel. The rated voltage should be 10 V or higher.

Table 14-1: Suggested effective value for DC-to-DC converter output capacitor (C_{VDDP})

Effective coil value (at maximum current)	Minimum effective capacitance (at the boost voltage)
1 µH	6 µF

14.1.2 Supply capacitor

C_{BST} can be about half the value of C_{VDDP}.

14.1.3 DC-to-DC converter inductor

An inductor is required at the output of the DC-to-DC converter (L_{BST}). For stability, the inductance of the coil should remain above 0.7 µH and below 1.2 µH under all conditions.

A DC-to-DC coil value of 1 µH or less is strongly recommended. If the coil value is increased, the value of the output capacitor will also need to be increased by at least the same factor. If the output capacitor is not large enough, the DC-to-DC converter will be unstable. The positioning of the output capacitor on the PCB is also critical. The capacitor must be located as close as possible to the TFA9890A and the connections between them should be on the top layer. A nominal value of 1 µH provides the optimum balance between current capability, component size and efficiency.

The choice of inductor is strongly influenced by the impedance of the speaker used in the application. The speaker impedance determines the output current of the DC-to-DC converter. The minimum required battery voltage, the boost voltage and the inductor value determine the peak inductor current (I_{LM}).

14.1.4 Reset pin (RST)

If the reset pin is not used, it is advised to connect it directly to ground. It has an internal pull-down resistance of 100 kΩ.

14.2 Application diagrams

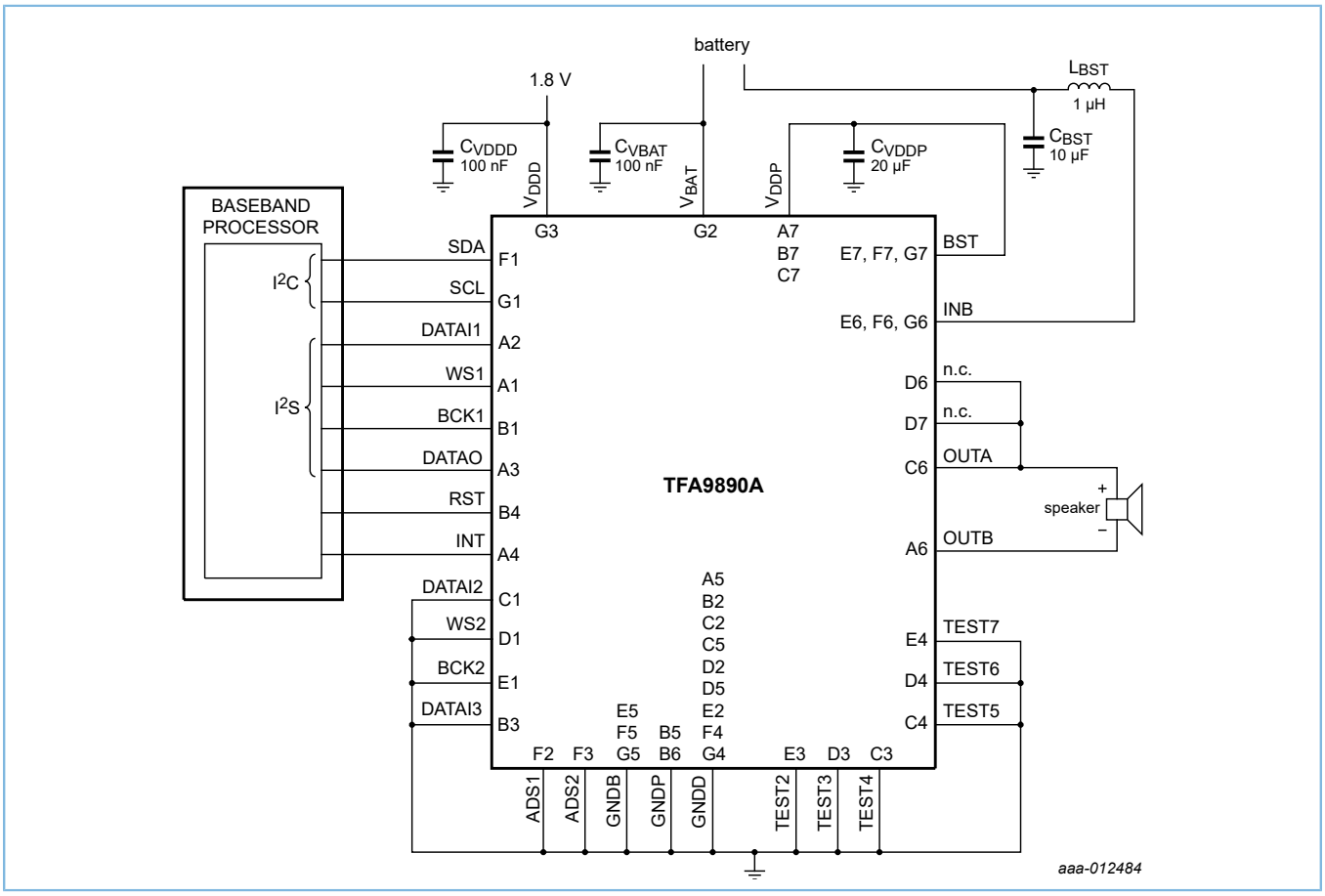


Figure 14-1: Typical mono application (simplified)

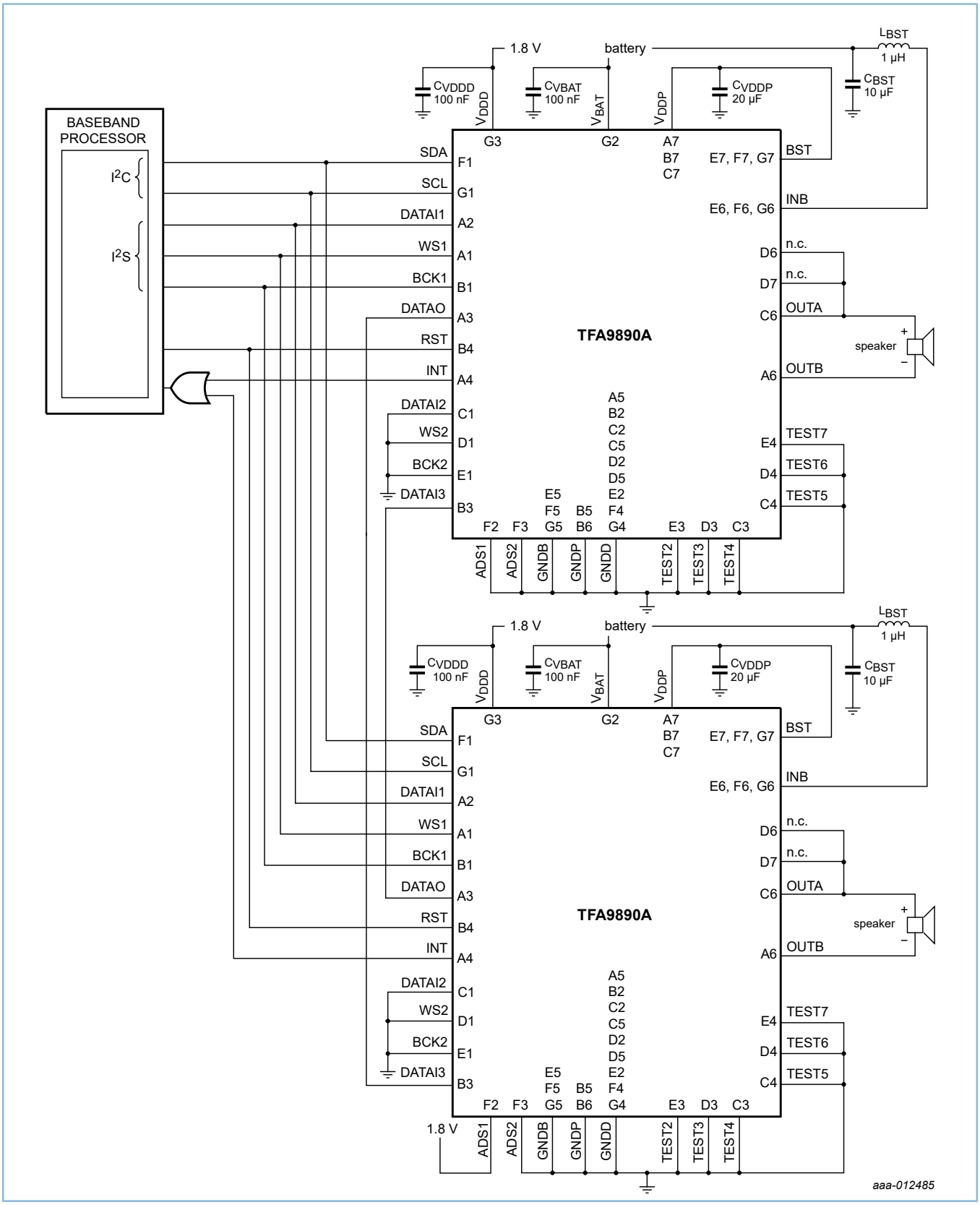


Figure 14-2: Typical stereo application (simplified)

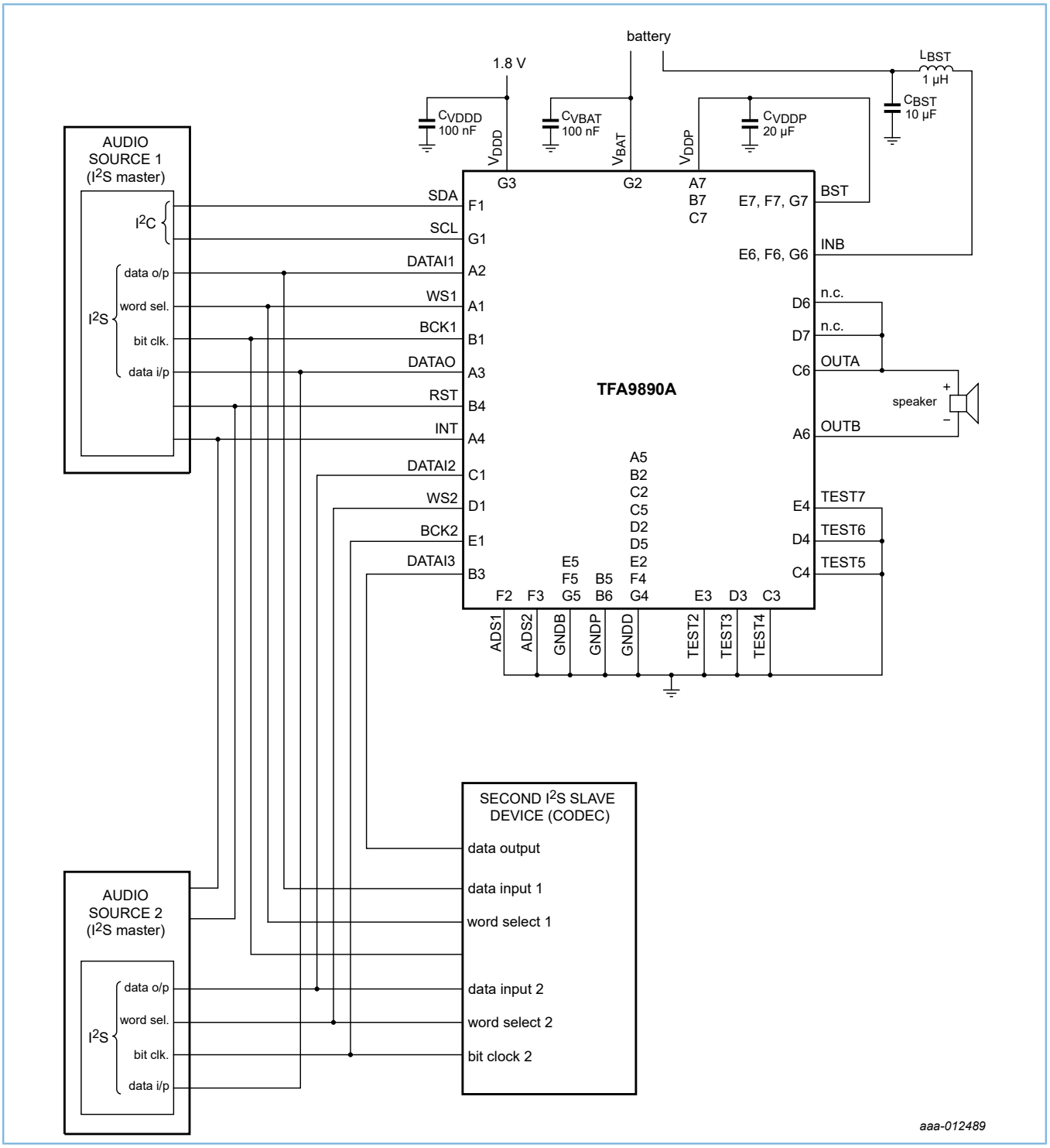
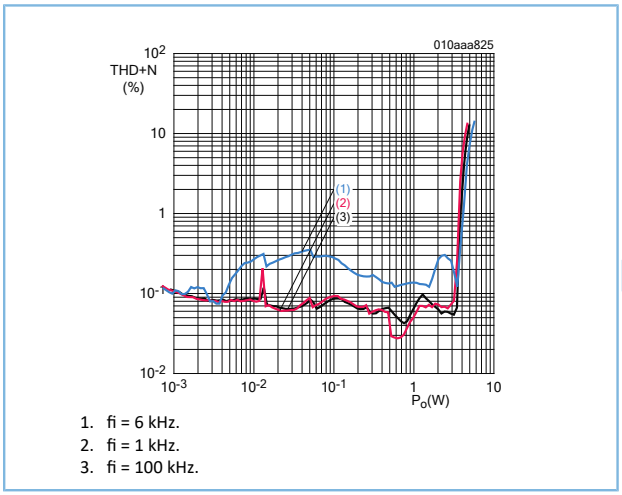


Figure 14-3: Typical mono application with two audio sources and a second I²S slave device

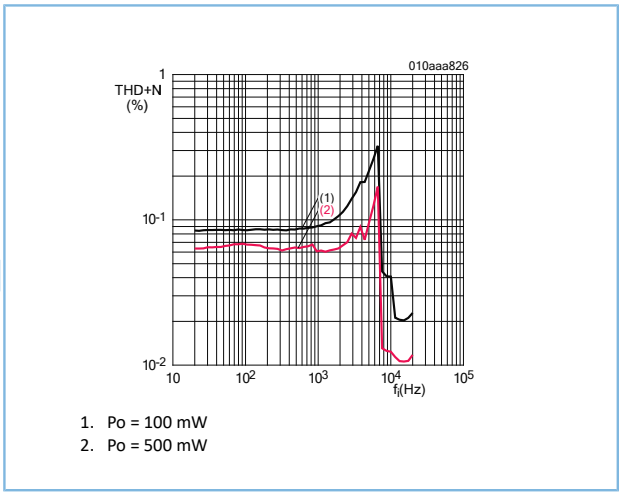
14.3 Curves measured in reference design (demonstration board)

All measurements were taken with V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V; L_{BST} = 1 µH; R_L = 8 Ω; L_L = 20 µH; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; CoolFlux DSP bypassed; default settings, unless otherwise specified.



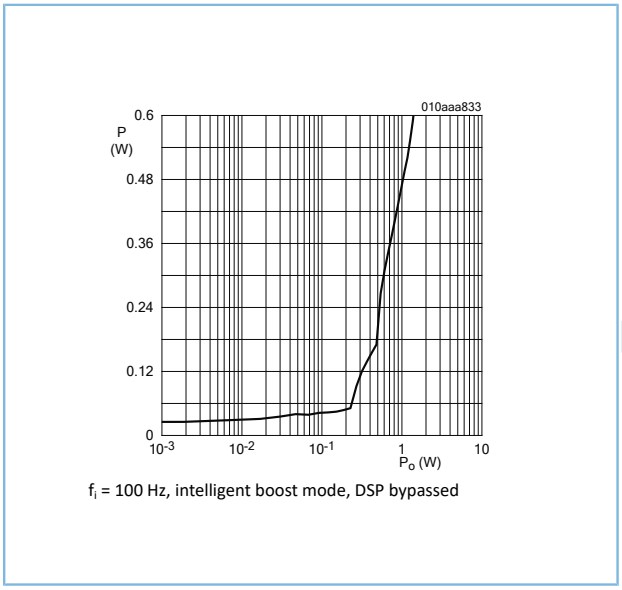
1. fi = 6 kHz.
2. fi = 1 kHz.
3. fi = 100 kHz.

Figure 14-4: THD plus noise as a function of output power



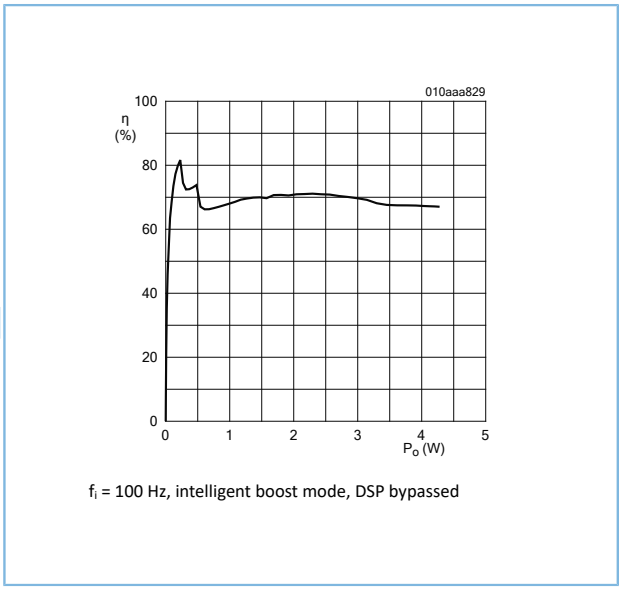
1. Po = 100 mW
2. Po = 500 mW

Figure 14-5: THD plus noise as a function of frequency



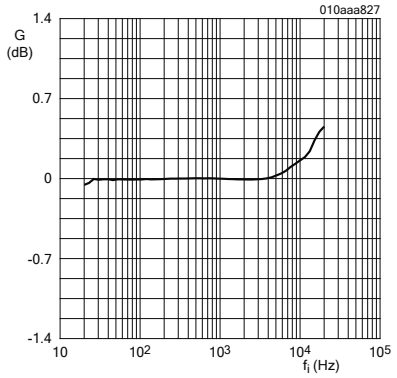
f_i = 100 Hz, intelligent boost mode, DSP bypassed

Figure 14-6: Power dissipation as a function of output power



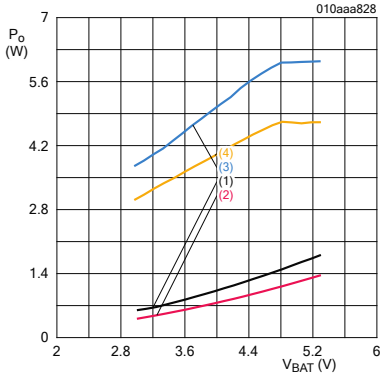
f_i = 100 Hz, intelligent boost mode, DSP bypassed

Figure 14-7: Efficiency as a function of output power



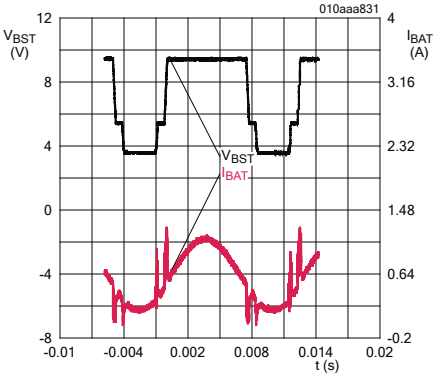
Po = 500 mW

Figure 14-8: Normalized gain as a function of frequency



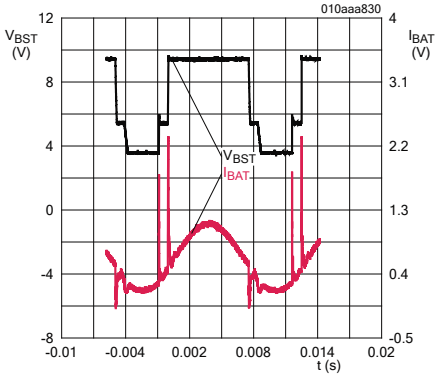
1. THD+N = 10 %, no boost (Follower mode)
2. THD+N = 1 %, no boost (Follower mode)
3. THD+N = 10 %, boost on
4. THD+N = 1 %, boost on

Figure 14-9: Output power as a function of battery supply voltage



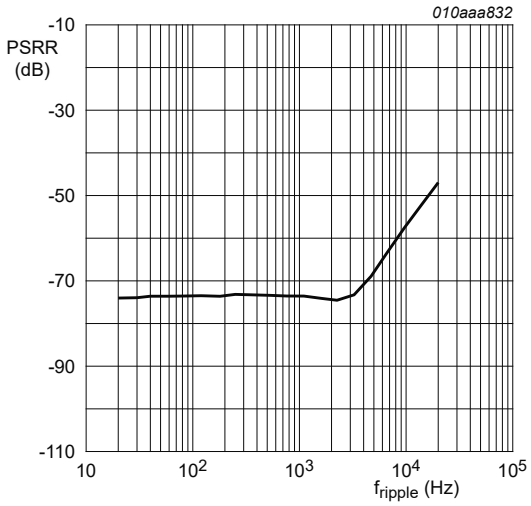
a. fast ramp-up

input signal is a sine wave; fi = 100 Hz



b. immediate ramp-up

Figure 14-10: DC-to-DC converter ramp-up behavior

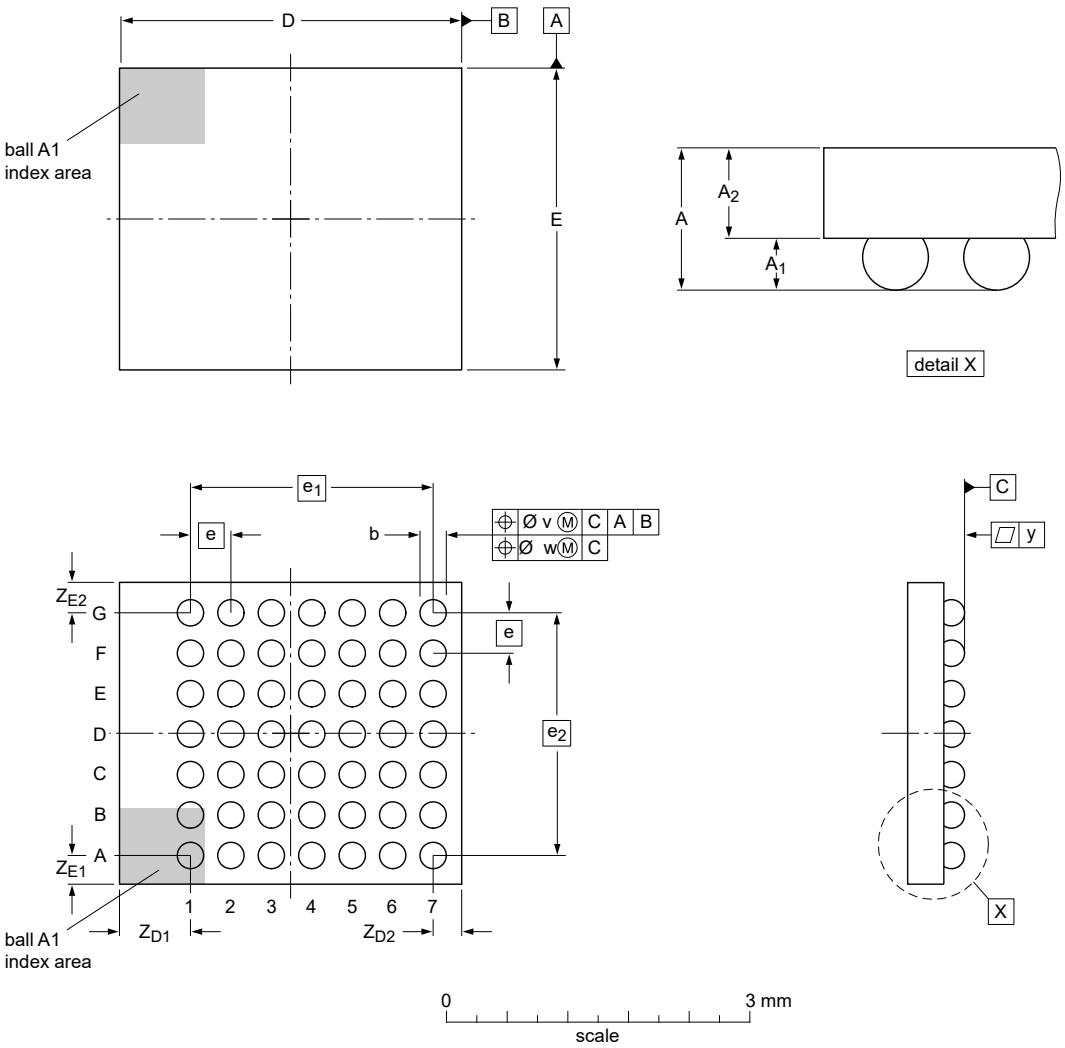


V_{ripple} = 200 mV(RMS) on V_{BAT}

Figure 14-11: PSRR as a function of ripple frequency

15 Package outline

WLCSP49: wafer level chip-size package;
49 bumps; 3.37 x 2.97 mm **TFA9890A**



Dimensions (mm are the original dimensions)

Unit		Amax	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}
	max	0.6	0.22	0.38	0.28	3.40	3.00							0.725	0.305	0.305	0.325
mm	nom		0.20	0.36	0.26	3.37	2.97	0.4	2.4	2.4	0.015	0.04	0.02	0.695	0.275	0.275	0.295
	min		0.18	0.34	0.24	3.34	2.94							0.665	0.245	0.245	0.265

wlcsp49_tfa9890a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
TFA9890A						~~13-05-17~~ 14-03-27

Figure 15-1: Package outline TFA9890A (WLCSP49)

16 Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

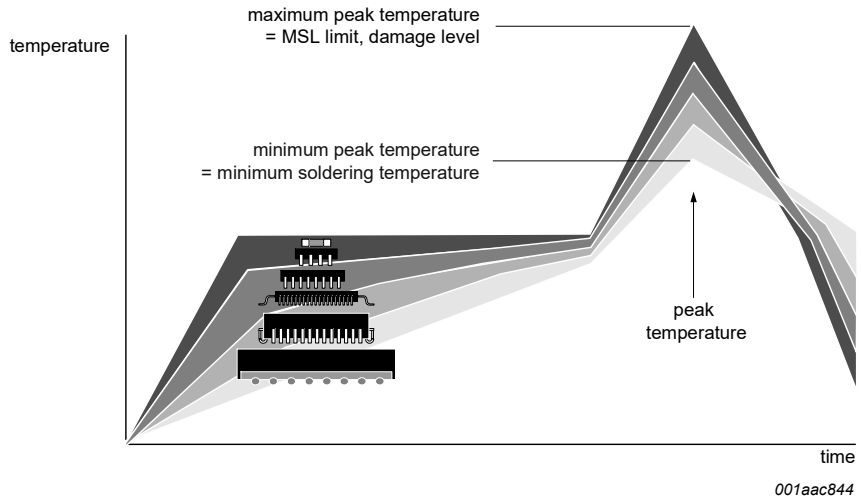
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16-1) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16-1.

Table 16-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16-1.



MSL: Moisture Sensitivity Level

Figure 16-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17 Legal and contact information

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18 Revision history

Table 18-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9890A_SDS v 3.1	20200420	Product short data sheet	-	TFA9890A_SDS v 3.0
Modifications:	• Added version number to the ordering information			
TFA9890A_SDS v 3.0	20200121	Product short data sheet	-	TFA9890A_SDS v.2
Modifications:	• Updated document format based on Goodix template			
TFA9890A_SDS v.2	<tbd>	Product short data sheet	-	TFA9890A_SDS v.1
Modifications:	• Table 4-1: measurement conditions changed for parameter $P_{o(RMS)}$ (CLIP = 1) • Section 8.2: text revised • Table 8-1: revised; table note section added • Table 9-1: corrected errors in equivalent circuits (pin A4 belongs with pin A3) • Table 13-2: measurement conditions changed for parameters $P_{o(RMS)}$, S/N (CLIP = 1)			
TFA9890A_SDS v.1	20140916	Product short data sheet	-	-