TFA9891_SDS

9.5 V Boosted Audio System with Adaptive Sound Maximizer and Speaker Protection

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Contents

1 General description

The TFA9891 is a high efficiency class-D audio amplifier with a sophisticated speaker boost and protection algorithm. It can deliver 7.2 W peak output power to an 8 Ω speaker, at a supply voltage of 3.6 V. The internal boost converter raises the supply voltage to 9.5 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9891 maximizes acoustic output while ensuring that the diaphragm displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures that the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker. An integrated Dynamic Range Compressor (DRC) allows the speaker to operate at the highest possible power rating without suffering physical damage.

Unlike competing solutions, the adaptive sound maximizer algorithm uses feedback to calculate both the temperature and the excursion. It allows the TFA9891 to adapt to changes in the acoustic environment.

Internal intelligent DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. It maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The TFA9891 also incorporates advanced battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery. Drawing excessive load currents from the battery could cause a system undervoltage. The advanced processor minimizes the impact of a falling battery voltage on the audio quality, by preventing distortion as the battery discharges.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The audio input interface is I^2S and the control settings are communicated via an I^2C-bus interface.

The device also provides the speaker with robust protection against ESD damage. In a typical application, no additional components are required to withstand a 15 kV discharge on the speaker.

The TFA9891 is available in a 49-bump WLCSP (Wafer Level Chip-Size Package) with a 400 µm pitch.

2 Features and benefits

- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
  - Fully embedded software, no additional license fee or porting required
  - Total integrated solution that includes DSP, amplifier, DC-to-DC, sensing and more
- Adaptive excursion control which guarantees that the speaker membrane excursion never exceeds its rated limit
- Multiband Dynamic Range Compressor (DRC) allows independent control of up to three frequency bands
- Audio enhancement
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker box leakage
- Output power: 3.6 W (RMS) into 8 Ω at 3.6 V supply voltage (THD = 1 %)
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Bandwidth extension option to increase low frequency response
- Compatible with standard acoustic echo canceler (s)
- High efficiency and low-power dissipation
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Two I^2S inputs to support two audio sources or one Pulse Density Modulation (PDM) input
- A third I^2S input dedicated to inter-chip communications
- I^2C-bus control interface (400 kHz)
- Speaker current and voltage monitoring (via the I^2S-bus or PDM output) for Acoustic Echo Cancellation (AEC) at the host
- Fully short-circuit proof across the load and to the supply lines
- Sample frequencies from 8 kHz to 48 kHz supported in I^2S mode and 16 kHz to 48 kHz in PDM mode
- 3-bit clock/word select ratios supported (32x, 48x, and 64x) in I^2S mode
- Bit clock speed from 2.048 MHz up to 6.144 MHz in PDM mode
- Option to route I^2S input directly to I^2S output allowing a second I^2S output slave device to be used in combination with TFA9891
- TDM interface supported (with limited functionality)
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- 15 kV system-level ESD protection without external components

3 Applications

- Mobile phones, Tablets
- Portable Navigation Devices (PND)
- Notebooks/netbooks
- MP3 players and portable media players
- Small audio systems

4 Quick reference data

Table 4-1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT	2.7	-	5.5	V
V_{DDD}	digital supply voltage	on pin VDDD	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin VBAT and in DC-to-DC converter coil; operating modes with load; DC-to-DC converter in adaptive boost mode (no output signal, V_{BAT} = 3.6 V, V_{DDD} = 1.8 V)	-	4	-	mA
		power-down mode	-	1	-	µA
I_{DDD}	digital supply current	on pin VDDD; operating modes; speaker boost protection activated	-	20	-	mA
		on pin VDDD; operating modes; CoolFlux DSP bypassed	-	7	-	mA
		on pin VDDD; power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V	-	10	-	µA
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; CLIP = 0				
		R_L = 8 Ω; f_s = 48 kHz	-	3.6	-	W
		R_L = 8 Ω; f_s = 32 kHz	-	3.7	-	W

5 Ordering information

Table 5-1: Ordering information

Type number	Package		
	Name	Description	Version
TFA9891UK	WLCSP49	wafer level chip-scale package; 49 bumps; 3.43 × 2.98 × 0.56 mm (backside coating included)	TFA9891

6 Block diagram

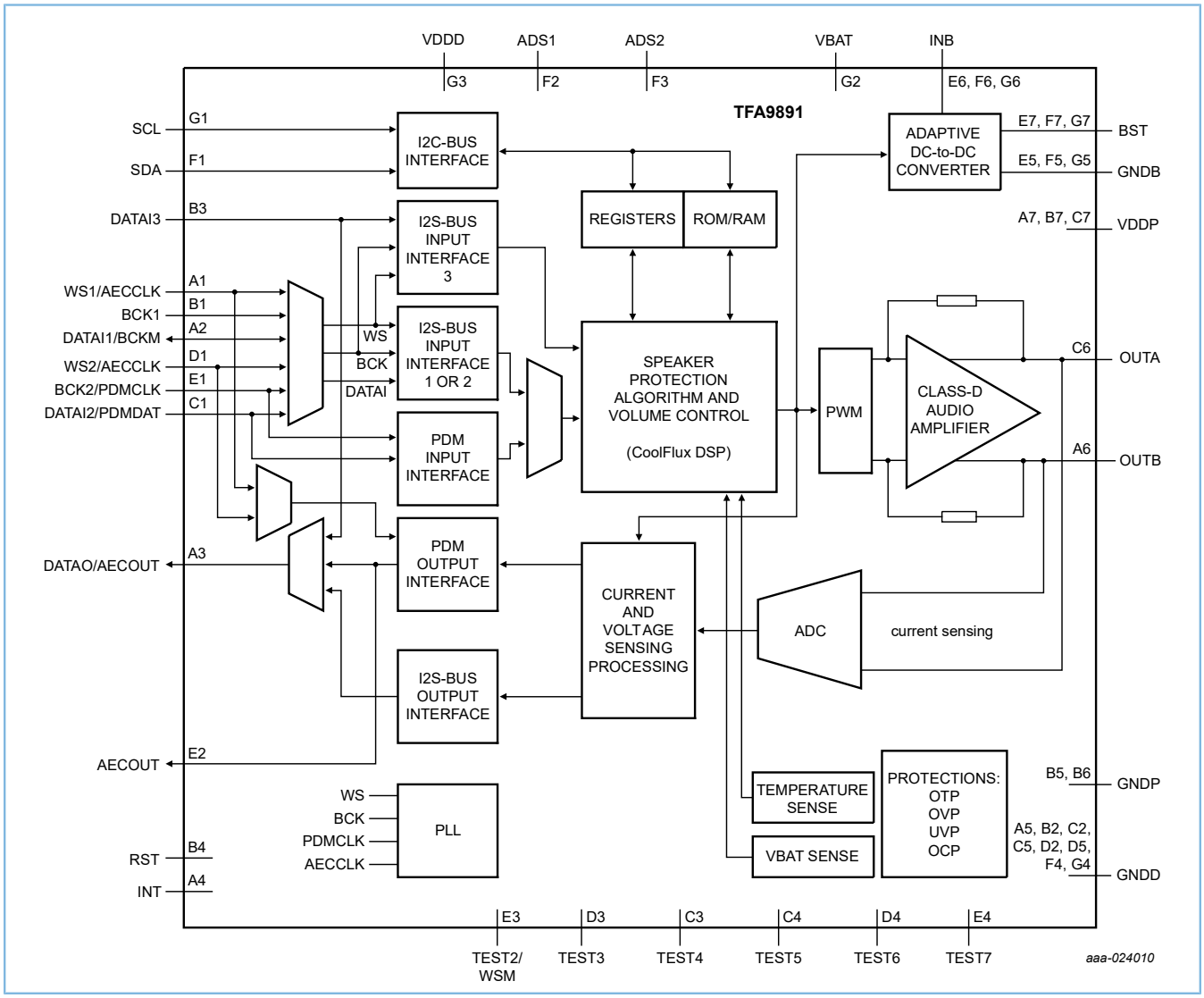
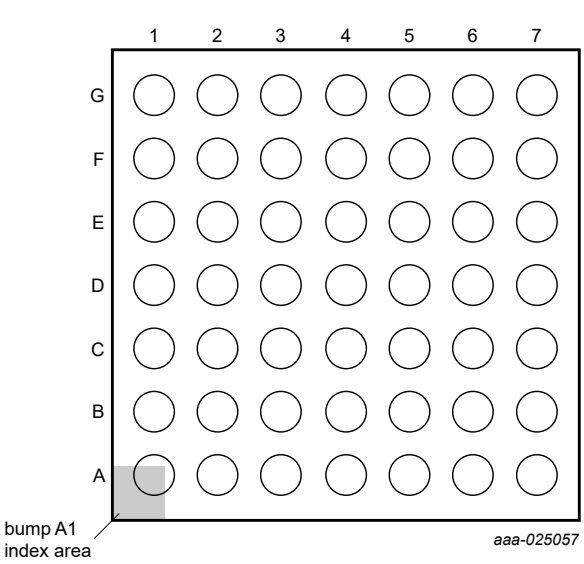


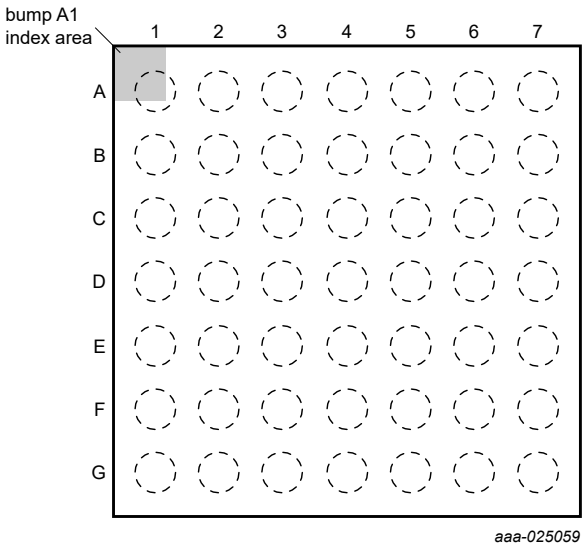
Figure 6-1: Block diagram

7 Pinning information

7.1 Pinning



a. Bottom View



b. Transparent top view

Figure 7-1: Bump configuration

	1	2	3	4	5	6	7
A	WS1/ AECCLK	DATAI1/ BCKM	DATAO/ AECOUT	INT	GNDD	OUTB	VDDP
B	BCK1	GNDD	DATAI3	RST	GNDP	GNDP	VDDP
C	DATAI2/ PDMDAT	GNDD	TEST4	TEST5	GNDD	OUTA	VDDP
D	WS2/ AECCLK	GNDD	TEST3	TEST6	GNDD	n.c.	n.c.
E	BCK2/ PDMCLK	AECOUT	TEST2/ WSM	TEST7	GNDB	INB	BST
F	SDA	ADS1	ADS2	GNDD	GNDB	INB	BST
G	SCL	VBAT	VDDD	GNDD	GNDB	INB	BST

aaa-024011

1. Transparent top view

Figure 7-2: Bump mapping

7.2 Pin description

Table 7-1: Pin description

Symbol	Pin	Type		Description
WS1/AECCLK	A1	I		I^2S mode: Digital audio word select input 1 for I^2S interface 1 PDM mode: PDM input clock used for AEC reference output (in mono)
DATAI1/BCKM	A2	I/O		I^2S mode: Digital audio data input 1 for I^2S interface 1 PDM mode: Master I^2S audio bit clock output for stereo gain exchange
DATAO/AECOUT	A3	O		I^2S mode: Digital audio data output PDM mode mono: AEC PDM output PDM mode stereo: Gain exchange between 2x devices
INT	A4	O		interrupt output
GNDD	A5	P		digital ground
OUTB	A6	O		inverting output
VDDP	A7	P		power supply voltage
BCK1	B1	I		digital audio bit clock input 1 for I^2S interface 1
GNDD	B2	P		digital ground
DATAI3	B3	I		digital audio data input 3 for I^2S interface 3
RST	B4	I		reset input
GNDP	B5	P		power ground
GNDP	B6	P		power ground
VDDP	B7	P		power supply voltage
DATAI2/PDMDAT	C1	I		I^2S mode: Digital audio data input 2 for I^2S interface 2 PDM mode: PDM audio data stream input
GNDD	C2	P		digital ground
TEST4	C3	O		test signal input 4; for test purposes only, connect to PCB ground
TEST5	C4	O		test signal input 5; for test purposes only, connect to PCB ground
GNDD	C5	P		digital ground
OUTA	C6	O		non-inverting output
VDDP	C7	P		power supply voltage

Symbol	Pin	Type		Description
WS2/AECCLK	D1	I		I^2S mode: Digital audio word select input 2 for I^2S interface 2 PDM mode: PDM input clock used for AEC reference output (in stereo)
GNDD	D2	P		digital ground
TEST3	D3	O		test signal input 3; for test purposes only, connect to PCB ground
TEST6	D4	O		test signal input 6; for test purposes only, connect to PCB ground
GNDD	D5	P		digital ground
n.c.	D6	-	[1]	not connected
n.c.	D7	-	[1]	not connected
BCK2/PDMCLK	E1	I		I^2S mode: Digital audio bit clock input 2 for I^2S interface 2 PDM mode: PDM clock input for audio data stream
AECOUT	E2	O		PDM stereo: AEC PDM output I^2S mode or PDM mono mode: Pin is tristated internally; must be tied to GNDD externally
TEST2/WSM	E3	O		I^2S mode: Test signal input 2; connect to PCB ground PDM mode: Master audio word select output for stereo gain exchange between 2x devices
TEST7	E4	O		test signal input 7; for test purposes only, connect to PCB ground
GNDB	E5	P		boosted ground
INB	E6	P		DC-to-DC boost converter input
BST	E7	O		boosted supply voltage output
SDA	F1	I/O		I^2C-bus data input/output
ADS1	F2	I		address select input 1
ADS2	F3	I		address select input 2
GNDD	F4	P		digital ground
GNDB	F5	P		boosted ground
INB	F6	P		DC-to-DC boost converter input
BST	F7	O		boosted supply voltage output
SCL	G1	I		I^2C-bus clock input
VBAT	G2	P		battery supply voltage sense input

Symbol	Pin	Type		Description
VDDD	G3	P		digital supply voltage
GNDD	G4	P		digital ground
GNDB	G5	P		boosted ground
INB	G6	P		DC-to-DC boost converter input
BST	G7	O		boosted supply voltage output

[1] Can be used to simplify routing to pin OUTA (see *Table 7-1*).

8 Functional description

The TFA9891 is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost protection algorithm. *Figure 6-1* is a block diagram of the TFA9891.

In I2S mode, TFA9891 contains three I^2S data inputs and one I^2S data output. Two of the I^2S inputs, DATAI1 and DATAI2, can be selected as the audio input stream. The third I^2S input, DATAI3, is provided to support stereo applications. The selected WS/BCK signal is used to internally clock DATAI3 (at the output of the MUX controlled by ISEL; see *Figure 6-1*).

A 'pass-through' option allows one of the I^2S input interfaces to be connected directly to the I^2S output. It allows I^2S output slave device such as codec connected in parallel with TFA9891 to be routed directly to the audio host via I^2S output.

In PDM mode, the TFA9891 features one PDM input interface for audio stream and one PDM output interface to provide AEC voltage or current reference. It also has one I^2S input (DATAI3) and one I^2S output interface (DATAO). In this mode, the I^2S input/output interfaces are dedicated to communication between two devices for gain and synchronization on stereo platforms.

Regardless of active mode (I^2S or PDM), the I^2S output signal on DATAO can be configured to transmit DSP output signal, amplifier output current information, DATAI3 left or right signal information (bypass) or amplifier gain information. The gain information can be used to facilitate communication between two devices in stereo applications.

A SpeakerBoost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core maximizes the acoustical output of the speaker. The algorithm also limits membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that the speaker membrane excursion never exceeds its rated limit, to accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to accuracy of ±10 °C. Furthermore, advanced signal processing ensures that the audio quality remains acceptable always.

The protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

Output sound pressure levels are boosted within given mechanical, thermal and quality limits. An optional bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high-quality music in quiet environments.

The frequency response of the TFA9891 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 8 are processed with 24-bit single precision.

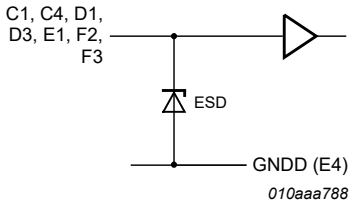
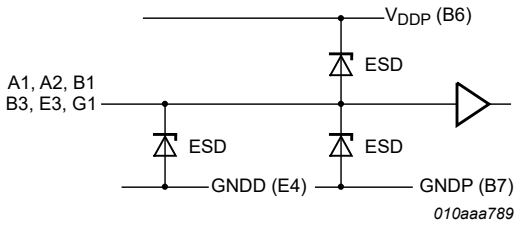
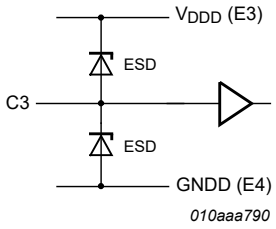
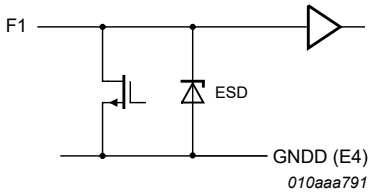
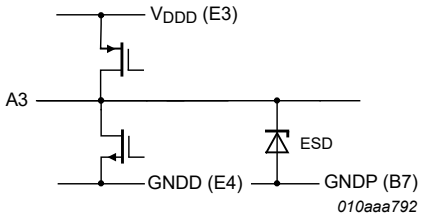
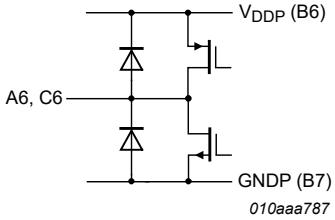
At low battery voltage levels, the gain is automatically reduced to limit battery current. The SpeakerBoost protection algorithm or the host application (external) controls the output volume. In the latter case, the boost features of the SpeakerBoost protection algorithm must be disabled to avoid neutralizing external volume control.

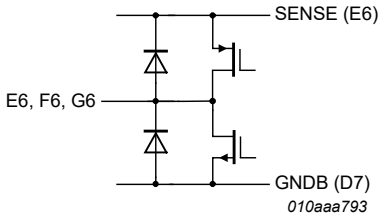
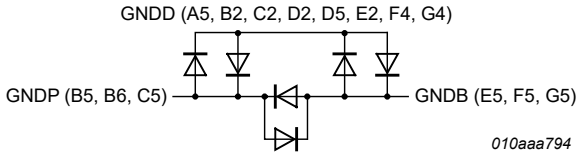
The SpeakerBoost protection algorithm output is converted into two pulse width modulated (PWM) signals which are injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the SpeakerBoost protection algorithm. It switches to follower mode ($V_{bst} = V_{BAT}$; no boost) when the audio output voltage is lower than the battery voltage.

9 Internal circuitry

Table 9-1: Internal circuitry

Pin	Symbol	Equivalent circuit
C1, C4, D1, D3, E1, F2, F3	DATAI2, TEST5, WS2, TEST3, BCK2, ADS1, ADS2	
A1, A2, A4, B1, B3, E3, G1	WS1, DATAI1, INT, BCK1, DATAI3, TEST2, SCL,	
C3	TEST4	
F1	SDA	
A3, E2	DATAO, AECOUT	
A6, C6	OUTB, OUTA	

Pin	Symbol	Equivalent circuit
E6, F6, G6	i.c.	
A5, B2, B5, B6, C2, C5, D2, D5, E5, F4, F5, G4, G5	GNDP, GNDB, GNDD	

10 I²C-bus interface and register settings

The TFA9891 supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control the TFA9891 and to transmit and receive data. The TFA9891 can only operate in I²C slave mode, as a slave receiver or as a slave transmitter.

10.1 TFA9891 addressing

The TFA9891 is accessed via an 8-bit code; see *Table 10-1*. Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address, as detailed in *Table 10-1*. The generic address is independent of pins ADS1 and ADS2.

Table 10-1: Address selection via pins ADS1 and ADS2

ADS2 pin voltage (V)	ADS1 pin voltage (V)	Address	Function
0	0	01101000	for write mode
		01101001	for read mode
0	V_{DDD}	01101010	for write mode
		01101011	for read mode
V_{DDD}	0	01101100	for write mode
		01101101	for read mode
V_{DDD}	V_{DDD}	01101110	for write mode
		01101111	for read mode
don't care	don't care	00011100 (generic address)	for write mode
don't care	don't care	00011101 (generic address)	for read mode

10.2 I²C-bus write cycle

The sequence of events that is followed when writing data to the I²C-bus registers of TFA9891 is specified in *Table 10-2*. 1 byte is transmitted at a time. Each register stores 2 bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

- The microcontroller asserts a start condition (S).
- The microcontroller transmits the 7-bit device address of the TFA9891, followed by the R/W bit set to 0.
- The TFA9891 asserts an acknowledge (A).
- The microcontroller transmits the 8-bit TFA9891 register address to which the first data byte is written.
- The TFA9891 asserts an acknowledge.

- The microcontroller transmits the first byte (the most significant byte).
- The TFA9891 asserts an acknowledge.
- The microcontroller transmits the second byte (the least significant byte).
- The TFA9891 asserts an acknowledge.
- The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address has been auto-incremented by the TFA9891.

Table 10-2: I²C-bus write cycle

Start	TFA9891 address	R/W	ACK	[1]	TFA9891 first register address	ACK	MSB	ACK	LSB	ACK	More data...	Stop
S	$01101A_2A_1$	0	A		ADDR	A	MS1	A	LS1	A	<....>	P

[1] ACK stands for acknowledge.

10.3 I²C-bus read cycle

The sequence of events that is followed when reading data from the I²C-bus registers of TFA9891 is specified in *Table 10-3*. 1 byte is transmitted at a time. Each of the registers stores 2 bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

- The microcontroller asserts a start condition (S)
- The microcontroller transmits the 7-bit device address of the TFA9891, followed by the R/W bit set to 0
- The TFA9891 asserts an acknowledge (A)
- The microcontroller transmits the 8 bit TFA9891 register address from which the first data byte is read
- The TFA9891 asserts an acknowledge
- The microcontroller asserts a repeated start (Sr)
- The microcontroller retransmits the device address followed by the R/W bit set to 1
- The TFA9891 asserts an acknowledge
- The TFA9891 transmits the first byte (the MSB)
- The microcontroller asserts an acknowledge
- The TFA9891 transmits the second byte (the LSB)
- The microcontroller asserts either an acknowledge or a negative acknowledge (NA)
    - If the microcontroller asserts an acknowledge, TFA9891auto increments the target register address and steps 9 to 12 are repeated

- If the microcontroller asserts a negative acknowledge, the TFA9891 frees the I²C-bus and the microcontroller generates a stop condition (P)

Table 10-3: I²C-bus read cycle

Start	TFA9891 address	R/W	ACK	First register address	ACK	Res	TFA9891 address	R/W	ACK	MSB	ACK	LSB	ACK	More data...	ACK	Stop
S	01101A_2A_1	0	A	ADDR	A	Sr	11011A_2A_1	1	A	MS1	A	LS1	A	<....>	NA	P

11 Limiting values

Table 11-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT	-0.3	+5.5	V
V_{bst}	boost voltage	on pin BST	-0.3	+11	V
V_{INB}	voltage on pin INB	on pin INB	-0.3	+11	V
V_{DDP}	power supply voltage	on pin VDDP	-0.3	+11	V
V_{DDD}	digital supply voltage	on pin VDDD	-0.3	+1.95	V
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	-2	+2	kV
		according to Charged Device Model (CDM)	-500	+500	V
Amplifier output					
V_O	output voltage	on pin OUTA and pin OUTB	-0.3	+11	V

12 Thermal characteristics

Table 12-1: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	four layer application board	40	60	K/W

13 Characteristics

13.1 I²C timing characteristics

Table 13-1: I²C-bus interface characteristics; see *Figure 13-1*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{bst} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter			0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.

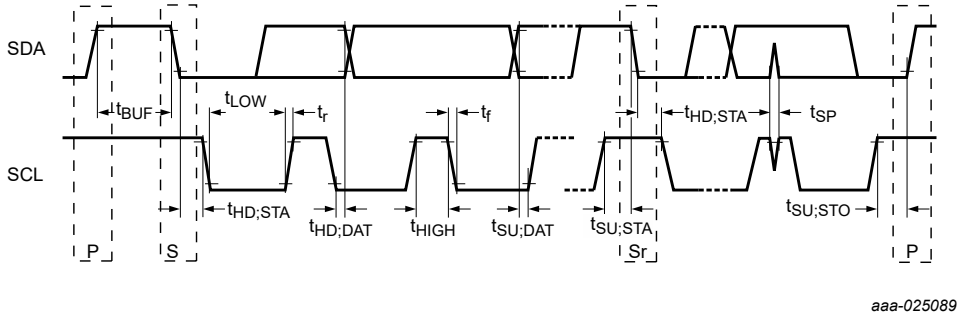


Figure 13-1: I²C timing

13.2 I²S timing characteristics

Table 13-2: I²S bus interface characteristics; see *Figure 13-2*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{bst} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin WS	[2]	8	-	48	kHz
f_{clk}	clock frequency	on pin BCK	[2]	32 × f_s	-	64 × f_s	Hz
t_{su}	set-up time	WS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to WS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] The I²S bit clock input (BCK) is used as a clock input for the DSP, as well as for the amplifier and the DC-to-DC converter. Both BCK and WS signals should be present for the clock to operate correctly.

[3] This parameter is not tested during production; design guarantees the value and is checked during product validation.

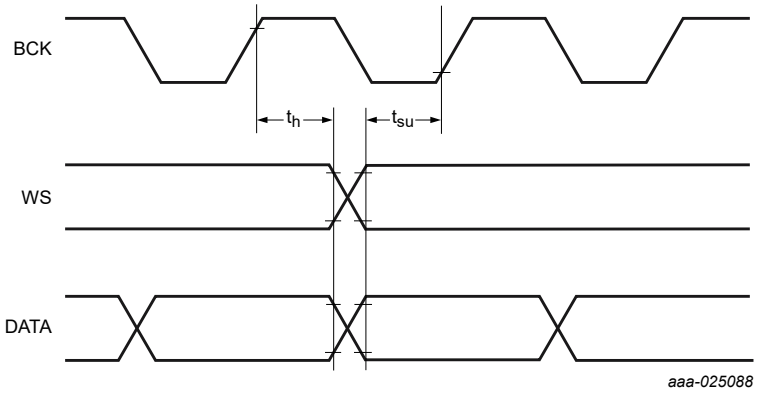
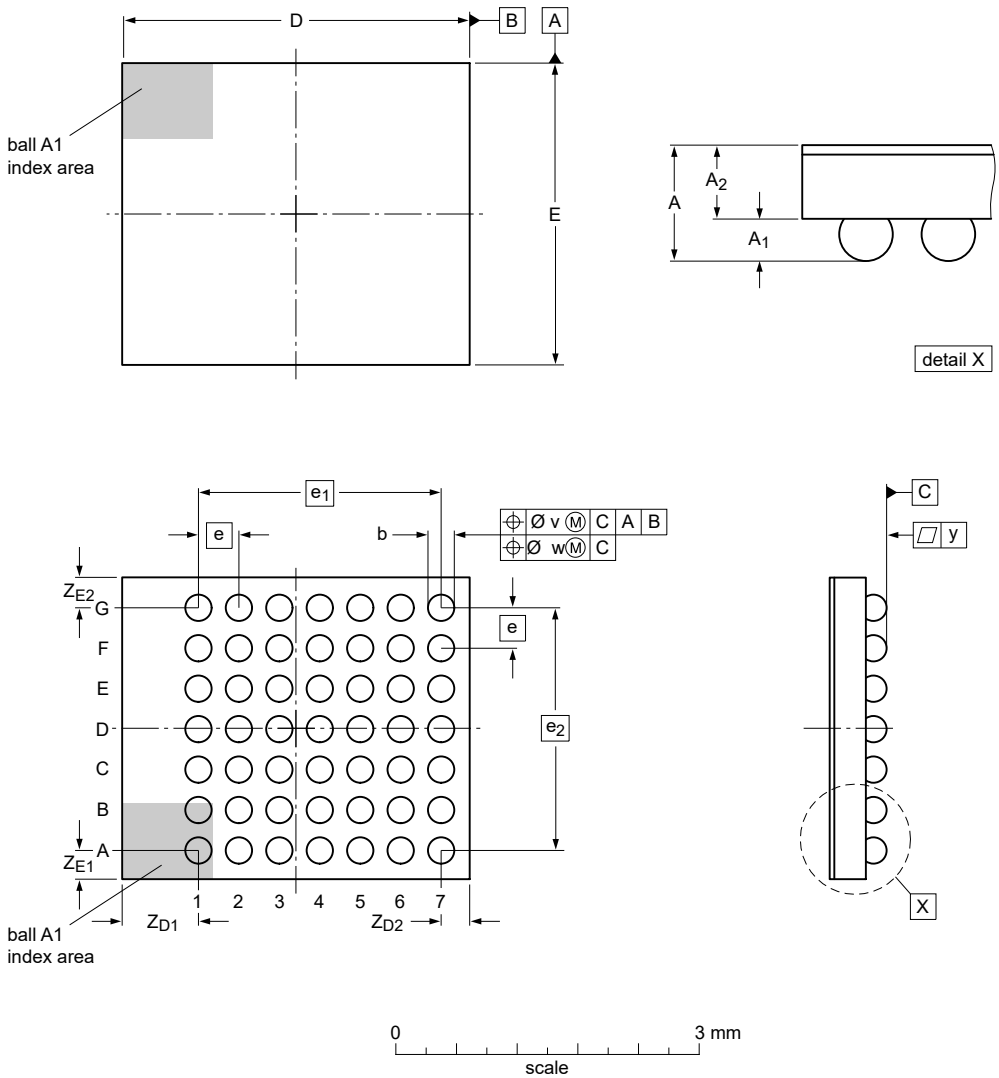


Figure 13-2: I^2S timing

14 Package outline

WLCSP49: wafer level chip-scale package; 49 bumps; 3.43 x 2.98 x 0.56 mm (Backside coating included) **TFA9891**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}
	max	0.60	0.23	0.385	0.29	3.46	3.01										
mm	nom	0.56	0.20	0.360	0.26	3.43	2.98	0.4	2.4	2.4	0.015	0.04	0.02	0.75	0.28	0.28	0.30
	min	0.52	0.17	0.335	0.23	3.40	2.95										

Note: Backside coating 40 µm

wlcsp49_tfa9891_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
TFA9891						~~15-07-21~~ 16-07-13

Figure 14-1: Package outline TFA9891 (WLCSP49)

15 Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

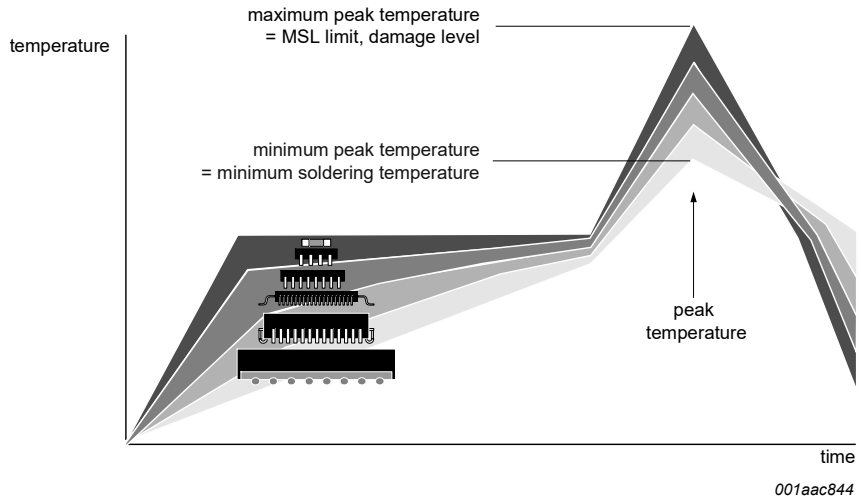
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see *Figure 15-1*) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with *Table 15-1*.

Table 15-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see *Figure 15-1*.



MSL: Moisture Sensitivity Level

Figure 15-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16 Abbreviations

Table 16-1: Abbreviations

Acronym	Description
AEC	Acoustic Echo Cancellation
API	Application Programming Interface
DRC	Dynamic Range Compressor
PLL	Phased Locked Loop
PND	Portable Navigation Devices
OSR	Over Sampling Ration
RPC	Remote Procedure Call
WLCSP	Wafer Level Chip-Size Package

17 Legal and contact information

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18 Revision history

Table 18-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9891_SDS v 2.0	20200121	Product short data sheet	-	TFA9891_SDS v.1
Modifications:	• Updated document format based on Goodix template			
TFA9891_SDS v.1	20161221	Product short data sheet	-	-