TFA9875_SDS

Version: 1.0

Release Date: 2021-11-17

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1 General description

The TFA9875 is a high efficiency boosted class-D audio amplifier. It can deliver up to 7.7 Wrms output power into an 8 Ω speaker. The device supports dual voice coil speaker protection by sensing the speaker current and the voltage over each voice coil (dual voltage sense).

The internal adaptive DC-to-DC converter raises the supply voltage up to 12 V, providing ample headroom for major improvements in sound quality. The supply voltage is only raised when necessary, maximizing the output power of the class-D audio amplifier while limiting quiescent power consumption.

The TFA9875 can be configured to drive either a hands-free speaker (6 Ω to 8 Ω) for audio playback or a receiver speaker (≤32 Ω), for handset playback. So, it can be embedded in platforms supporting both a hands-free speaker and a handset speaker. The maximum output power and the noise levels are lower in handset call use case than in hands-free call use case.

The audio interface is TDM and the control settings are communicated via the I^2C interface.

The TFA9875 is available in a 36-bump wafer level chip-size package (WLCSP) with a 400 µm pitch.

2 Features and benefits

- High output power: 7.7 W (average) into 8 Ω at 4.2 V supply voltage (THD = 1 %)
- Supports handset and hands-free speaker configurations
- Low noise: 10 µV mode in handset speaker configuration
- High efficiency, low power dissipation speaker driver
- Supports dual coil speaker protection, speaker current and two voltage sense circuitries integrated
- Adaptive DC-to-DC converter increases the supply voltage smoothly when switching between fixed boost and adaptive boost modes, preventing that large battery supply spikes and limiting quiescent power consumption occur.
- Suppresses acoustical noise of the boost converter decoupling capacitor when the adaptive DC-to-DC converter is active
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- I^2C-bus control interface (400 kHz)
- TDM audio interface
- 16 kHz/32 kHz/44.1 kHz/48 kHz/96 kHz sample frequencies supported
- Programmable interrupt control via a dedicated interrupt pin
- Low RF susceptibility
- Overtemperature protection
- 8 kV system-level ESD protection without external components on amplifier output

3 Applications

- Mobile phones and tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks

4 Quick reference data

Table 4-1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD} in application		2.7	-	5.5	V
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V
V_{DDP}	power supply voltage	on pin VDDP		2.7	-	12.2	V
I_{BAT}	battery supply current on VBAT pin	normal power mode; operating mode with load R_L = 8 Ω; P_o = 380 mW, (average music power), V_{BAT} = 3.8 V; V_{BST} = 12 V		-	126	-	mA
		normal power mode, amplifier switching; input signal detection active; P_o = 0 mW; V_{BAT} = 3.8 V		-	5.8	-	mA
		idle power mode; input signal detection active; P_o = 0 mW; V_{BAT} = 3.8 V		-	55	-	µA
		power-down state		-	1	-	µA
I_{DDD}	digital supply current on VDDD pin	normal power mode; operating mode with load R_L = 8 Ω; P_o = 380 mW, (average music power); V_{DDD} = 1.8 V		-	5.75	-	mA
		normal power mode; amplifier switching; input signal detection active; P_o = 0 mW; V_{DDD} = 1.8 V		-	5.75	-	mA
		idle power mode; active signal level detection; P_o = 0 mW; V_{DDD} = 1.8 V		-	1.65	-	mA
		power-down state		-	1	30	µA
R_L	load resistance			6	-	38	Ω
$P_{o(AV)}$	average output power	THD+N = 1 %; (R_L = 8 Ω; L_L = 44 µH); V_{BST} = 12.0 V; V_{BAT} = 4.2 V; V_{DDD} = 1.8 V		-	7.7	-	W
$V_{n(o)}$	output noise voltage	A-weighted; no input signal; low-noise mode; f_s = 48 kHz		-	10	-	µV

5 Ordering information

Table 5-1: Ordering information

Type number	Package	
	Name	Description
TFA9875AUK/N1	WLCSP36	wafer level chip-scale package; 36 bumps; 0.4 mm pitch,
TFA9875CUK/N1	WLCSP36	wafer level chip-scale package; 36 bumps; 0.4 mm pitch, back side coating

6 Block diagram

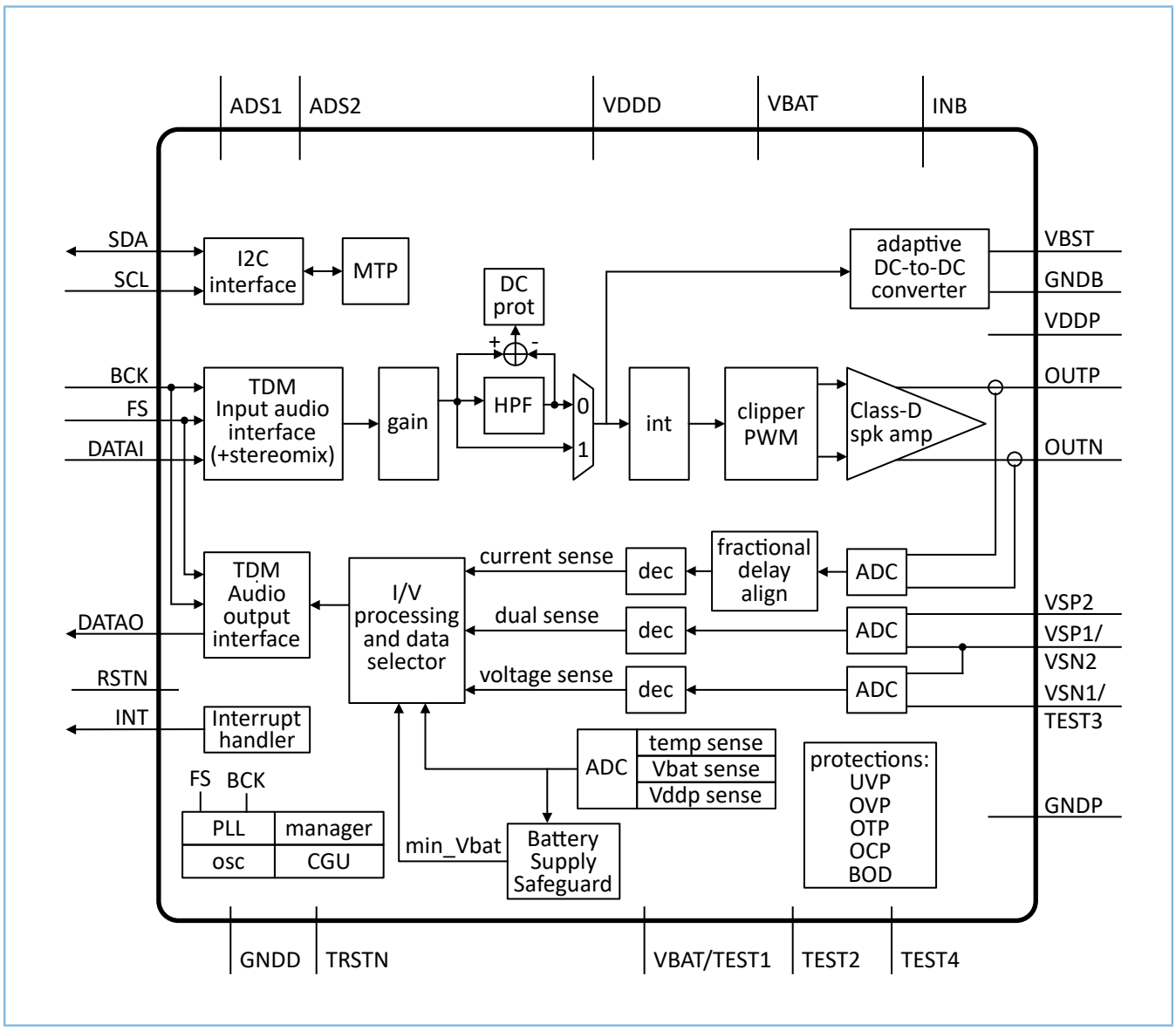


Figure 6-1: Block diagram

7 Pinning information

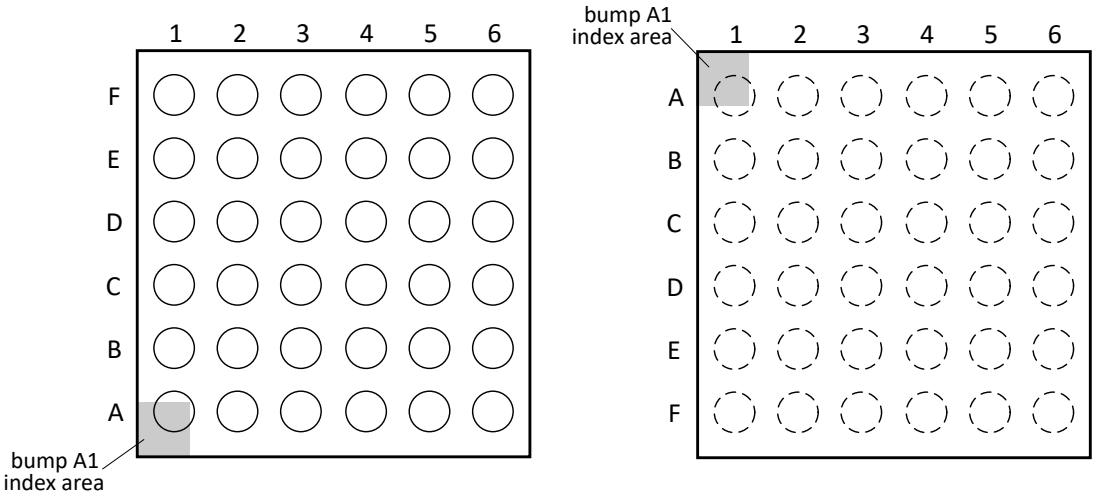


Figure 7-1: Bump configuration

	1	2	3	4	5	6
A	RSTN	BCK	FS	SCL	SDA	TRSTN
B	DATAO	DATAI	ADS2	ADS1	INT	VDDD
C	VBAT	TEST1	VSN1/ TEST3	TEST2	VSN2/ VSP1	VSP2
D	GNDB	GNDB	GNDB	GNDP	GNDP	GNDD
E	INB	INB	INB	TEST4	OUTP	OUTN
F	VBST	VBST	VBST	VDDP	VDDP	VDDP

Transparent top view

Figure 7-2: Bump mapping

Table 7-1: Pinning

Symbol	Pin	Type	Description
RSTN	A1	I	active low reset input
BCK	A2	I	digital audio bit clock input for TDM interface
FS	A3	I	digital audio frame sync input for TDM interface
SCL	A4	I	I^2C-bus clock input

Symbol	Pin	Type	Description
SDA	A5	I/O	I^2C-bus data input/output
TRSTN	A6	I	test signal input TRSTN, connect to PCB ground
DATAO	B1	O	digital audio data output for TDM interface
DATAI	B2	I	digital audio data input for TDM interface
ADS2	B3	I	digital I^2C address select input 2
ADS1	B4	I	digital I^2C address select input 1
INT	B5	O	digital interrupt output
VDDD	B6	P	digital supply voltage
VBAT	C1	P	battery supply voltage
TEST1	C2	P	test signal input 1; for test purposes only; connect to VBAT
VSN1/TEST3	C3	I	voltage sense 1 negative input
TEST2	C4	I	test signal input 2; for test purposes only; connect to PCB ground, or connect via a capacitor to PCB ground
VSP1/VSN2	C5	I	voltage sense 1 positive input and voltage sense 2 negative input
VSP2	C6	I	voltage sense 2 positive input
GNDB	D1	P	booster ground
GNDB	D2	P	booster ground
GNDB	D3	P	booster ground
GNDP	D4	P	power ground
GNDP	D5	P	power ground
GNDD	D6	P	digital ground
INB	E1	P	DC-to-DC boost converter input
INB	E2	P	DC-to-DC boost converter input
INB	E3	P	DC-to-DC boost converter input
TEST4	E4	I	test signal input 4; for test purposes only; connect to PCB ground, or connect via a capacitor to PCB ground
OUTP	E5	O	non-inverting output
OUTN	E6	O	inverting output
VBST	F1	O	boosted supply voltage output

Symbol	Pin	Type	Description
VBST	F2	O	boosted supply voltage output
VBST	F3	O	boosted supply voltage output
VDDP	F4	P	power supply voltage
VDDP	F5	P	power supply voltage
VDDP	F6	P	power supply voltage

8 Functional description

The TFA9875 is a highly efficient bridge tied load (BTL) class-D audio amplifier as depicted in block diagram (see Figure 6-1).

TFA9875 contains an I^2C and I^2S / TDM audio interface for communicating with the audio host. The device is able to mix an incoming stereo stream into a mono signal.

The digital audio stream is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the output voltage to the level that the class-D amplifier requires.

At low battery voltage levels, the maximum output level is automatically reduced to limit battery current (when battery supply safeguard is enabled).

9 Limiting values

Table 9-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT	−0.3	+6	V
V_{BST}	booster output voltage	on pin VBST	−0.3	+13 [1]	V
V_{INB}	booster input voltage	on pin INB	−0.3	V_{BST} + 0.3 [1]	V
V_{DDP}	power supply voltage	on pin VDDP	−0.3	+13 [1]	V
V_O	output voltage	on speaker connections; pins OUTP and OUTN	−0.3	V_{DDP} + 0.3[1]	V
V_{sense}	sense voltage	sense input voltage on pins VSN and VSP	−0.3	V_{DDP} + 0.3[1]	V
V_{DDD}	digital supply voltage	on pin VDDD	−0.3	+2.5	V
V_{low}	low voltage	on pins TEST1/TEST2	−0.3	V_{BAT} + 0.3	V
T_j	junction temperature		-	125	°C
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to human body model (HBM)	−2	+2	kV
		according to charge device model (CDM)	−500	+500	V

[1] Using the Goodix demo board, with a 1 mm wire/PCB track length on INB pin, AC pulses between −6 V and +18 V can be observed without damaging the device. These spikes do not end up inside the actual device.

10 Thermal characteristics

Table 10-1: Primary states selection

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	45	K/W

11 Characteristics

11.1 DC characteristics

Table 11-1: DC characteristics

All parameters are guaranteed for V_{BAT} = 3.8 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 12 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 30 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; DCMCC = 1111b; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD} in application		2.7	-	5.5	V
V_{DDP}	power supply voltage	on pin VDDP		2.7	-	12.2	V
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V
I_{BAT} + I_{INB}	battery supply current	normal power mode; P_o = 380 mW, (average music power)		-	126	-	mA
		normal power mode, amplifier switching; input signal detection active; P_o = 0 mW;		-	5.8	-	mA
		idle power mode; amplifier ready to receive signal; input signal detection active; P_o = 0 mW;		-	55	-	µA
		power-down state	[1]	-	1	-	µA
I_{DDD}	digital supply current on VDDD pin	normal power mode; P_o = 380 mW, (average music power);		-	5.75	-	mA
		normal power mode; amplifier switching; input signal detection active; P_o = 0 mW;		-	5.75	-	mA
		idle power mode; amplifier ready to receive signal; active signal level detection; P_o = 0 mW;		-	1.65	-	mA
		power-down state		-	1	30	µA
Pins FS, BCK, DATAI, ADS1, ADS2, SCL, SDA, RSTN							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDD}$	V
R_{pu}	pull-up resistance	pin RSTN		-	20	-	kΩ
C_{in}	input capacitance	pins FS, BCK, DATAI, ADS1, ADS2 and RSTN	[2]	-	-	5	pF
		pins SCL and SDA	[2]	-	-	10	pF
I_{LI}	input leakage current	1.8 V on pins FS, BCK, DATAI, ADS1 and ADS2		-	-	0.1	µA
		1.8 V on pins SCL and SDA		-	-	0.5	µA
Pins DATAO, INT, push-pull output stages							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DDD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins SDA, open-drain outputs, external resistor to V_{DDD}							
V_{OH}	HIGH-level output voltage			V_{DDD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA		-	-	400	mV
Pins OUTP, OUTN							
R_{DSon}	drain-source on-state resistance	PMOS + NMOS transistors		-	430	520	mΩ
Protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	-	°C
$V_{ovp(VBAT)}$	overvoltage protection on pin VBAT			5.6	-	6.0	V
$V_{uvp(VBAT)}$	undervoltage protection on pin VBAT			2.3	-	2.7	V
$I_{O(ocp)}$	overcurrent protection output current			2.5	-	-	A
DC-to-DC converter							
V_{BST}	voltage on pin VBST	DCVOS = 11110000; boost mode (after trim)	[3]	11.8	12	12.2	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.

[3] Boost switching frequency = 2 MHz in PWM mode.

11.2 AC characteristics

Table 11-2: AC characteristics

All parameters are guaranteed for V_{BAT} = 3.8 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 12 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 30 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; DCMCC = 1111b; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(AV)}$	average output power	hands-free speaker; THD+N = 1 %; using 4-layer application board; $R_{th(j-a)}$ = 42 K/W					
		R_L = 8 Ω;		-	7	-	W
		R_L = 8 Ω; V_{BAT} = 4.2 V		-	7.7	-	W
		R_L = 6 Ω; L_L = 30 µH) V_{BST} = 10.0 V; V_{BAT} = 3.8 V;		-	7	-	W
		R_L = 6 Ω; L_L = 30 µH) V_{BST} = 10.0 V; V_{BAT} = 4.2 V		-	7.8	-	W
		receiver speaker; THD+N = 1 %;					
		R_L = 32 Ω; voice mode		-	0.2	-	W
		R_L = 32 Ω; audio mode		-	2.1	-	W
Amplifier output pins (OUTP and OUTN)							
$\lvert V_{O(offset)} \rvert$	output offset voltage	DC-to-DC in follower mode		-	-	0.8	mV
Amplifier performances							
η_{po}	output power efficiency	on pin VBAT; P_o = 380 mW (average music power);	[2]	-	79	-	%
		on pin VBAT; P_o = 600 mW	[2]	-	86	-	%
		on pin V_{BAT}; P_o = 3 W	[2]	-	82	-	%
THD+N	total harmonic distortion-plus-noise	V_{DDP} > 9 V; P_o = 2.0 W;	[3]	-	-	0.05	%
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; normal mode; f_s = 48 kHz, or 96 kHz	[3]	-	35	-	µV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		a-weighted; no input signal; normal mode; f_s = 16 kHz, 32 kHz or 44.1 kHz	[3]	-	44	-	µV
		a-weighted; no input signal; low-noise mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, or 96 kHz	[3]	-	10	-	µV
		a-weighted; no input signal; idle power mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, or 96 kHz	[3]	-	1	-	µV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %); output noise voltage ($V_{n(o)}$); -60dBFS signal applied; low-noise mode; idle power mode disabled	[3]	110	116	-	dB
S/N	signal-to-noise ratio	a-weighted; V_{BAT} = 3.4 V to 5 V; maximum signal at THD = 1 %	[3]	-	116	-	dB
PSRR	power supply rejection ratio	from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}) f_{ripple} = 217 Hz square wave; V_{ripple} = 500 $mV_{(p-p)}$; P_o = 0; idle-power mode on; low-noise mode on		-	90	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 20 Hz to 1 kHz sine wave; V_{ripple} = 200 mV (RMS); P_o = 0; low-noise mode on		60	80	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 1 kHz to 20 kHz sine wave; V_{ripple} = 200 mV (RMS); P_o = 0; low-noise mode on		55	60	-	dB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔG/Δf	gain variation with frequency	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V		−0.2	-	+0.7	dB
V_{POP}	pop noise voltage	P_o = 0; DC-to-DC in follower mode		-	-	2	mV
R_L	load resistance			6	8	38	Ω
C_L	load capacitance	Output to ground		-	-	1	nF
f_{sw}	switching frequency	f_s = 16 kHz, 32 kHz, 48 kHz, or 96 kHz		-	384	-	kHz
		f_s = 44.1 kHz		-	352.8	-	kHz
$G_{(TDM-VO)}$	TDM to V_O gain	INPLEV = 0 dB; reference 0dBFS = 1V (RMS), TDMSPKG = 2 (typical)		6	19	21	dB
Amplifier power-up, power-down, and propagation delays							
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK;		-	2	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time			-	55	-	µs
$t_{d(off)}$	turn-off delay time			-	115	-	µs
$t_{d(alarm)}$	alarm delay time			-	190	-	ms
t_{PD}	propagation delay	f_s = 16 kHz	[4]	-	980	1100	µs
		f_s = 32 kHz	[4]	-	730	850	µs
		f_s = 44.1 kHz	[4]	-	680	800	µs
		f_s = 48 kHz	[4]	-	670	750	µs
		f_s = 96 kHz	[4]	-	600	700	µs
Booster inductance							
L_{bst}	boost inductance	Saturation current > 5.5A. L_{bst}not to degradate below minimum value at full rated current		0.7	1.0	1.2	µH
Voltage sensing and current sensing performance							
S/N	signal-to-noise ratio	I_O = 1.1 A (peak); a-weighted		62	65	-	dB
$\Delta V_{sense}/I_{sense}$	V_{sense}/I_{sense} ratio mismatch	pilot tone: −40 dBFS; pilot tone < 20 Hz	[5]	-	1	-	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD+N	total harmonic distortion-plus-noise	f_i = 20 Hz to 20 kHz; V_i = −12 dBFS		-	-	0.75	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.
[3] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance (speaker).
[4] delta propagation delay between left and right in stereo application = 0.1/f_s
[5] Intended for Speaker protection. In combination with Goodix Speaker protection, a speaker temperature accuracy of ± 10 °C can be realized.

11.3 TDM timing characteristics

Table 11-3: TDM bus interface characteristics

All parameters are guaranteed for V_{BAT} = 3.8 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 12 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 30 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; DCMCC = 1111b; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin FS	[2]	16	-	96	kHz
f_{clk}	clock frequency	on pin BCK	[2]	32f_s	-	12288	kHz
t_{su}	set-up time	FS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to FS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns
t_J	external clock jitter	PLL locked on FS	[4]	-	-	20	ns
		PLL locked on BCK	[4]	-	-	2	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. The BCK and WS signals must be present for the clock to operate correctly.
[3] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.

[4] When the PLL is locked on FS, the system is less sensitive to jitter, and noise performance can be guaranteed.

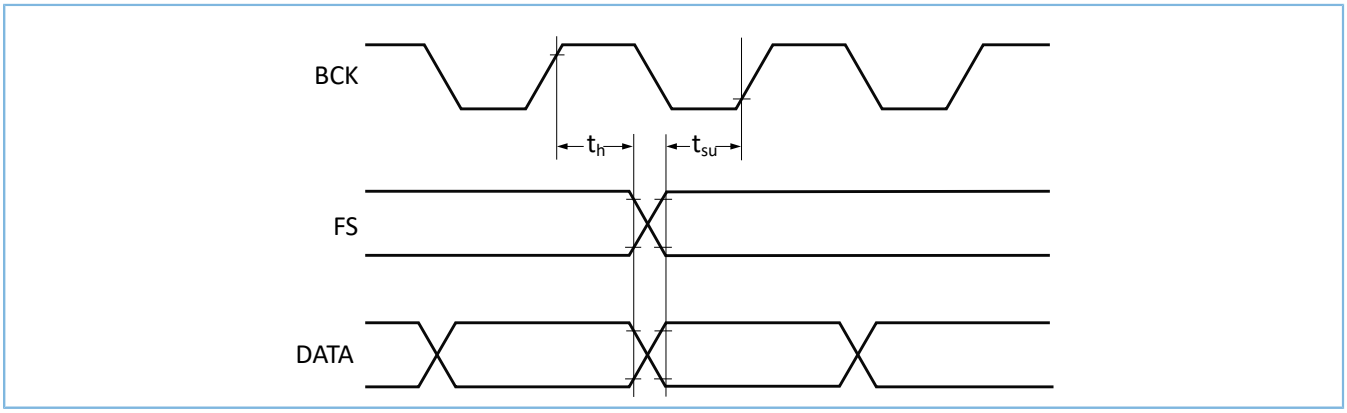


Figure 11-1: TDM timing

11.4 I²C timing characteristics

Table 11-4: I²C-bus interface characteristics

All parameters are guaranteed for V_{BAT} = 3.8 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 12 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 30 µH[1]; f_i = 1 kHz; f_s = 48 kHz; DCMCC = 1111b; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	$20 + 0.1C_b$	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	$20 + 0.1C_b$	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

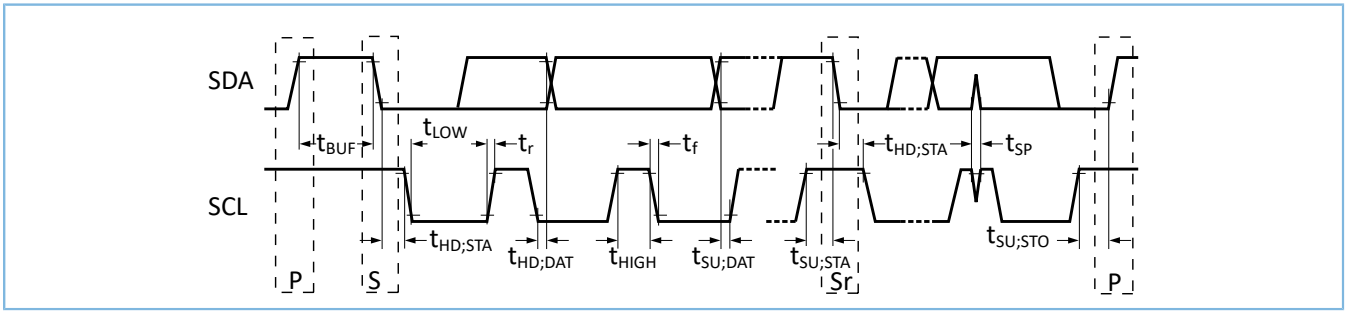


Figure 11-2: I²C timing

12 Application information

12.1 Application diagrams

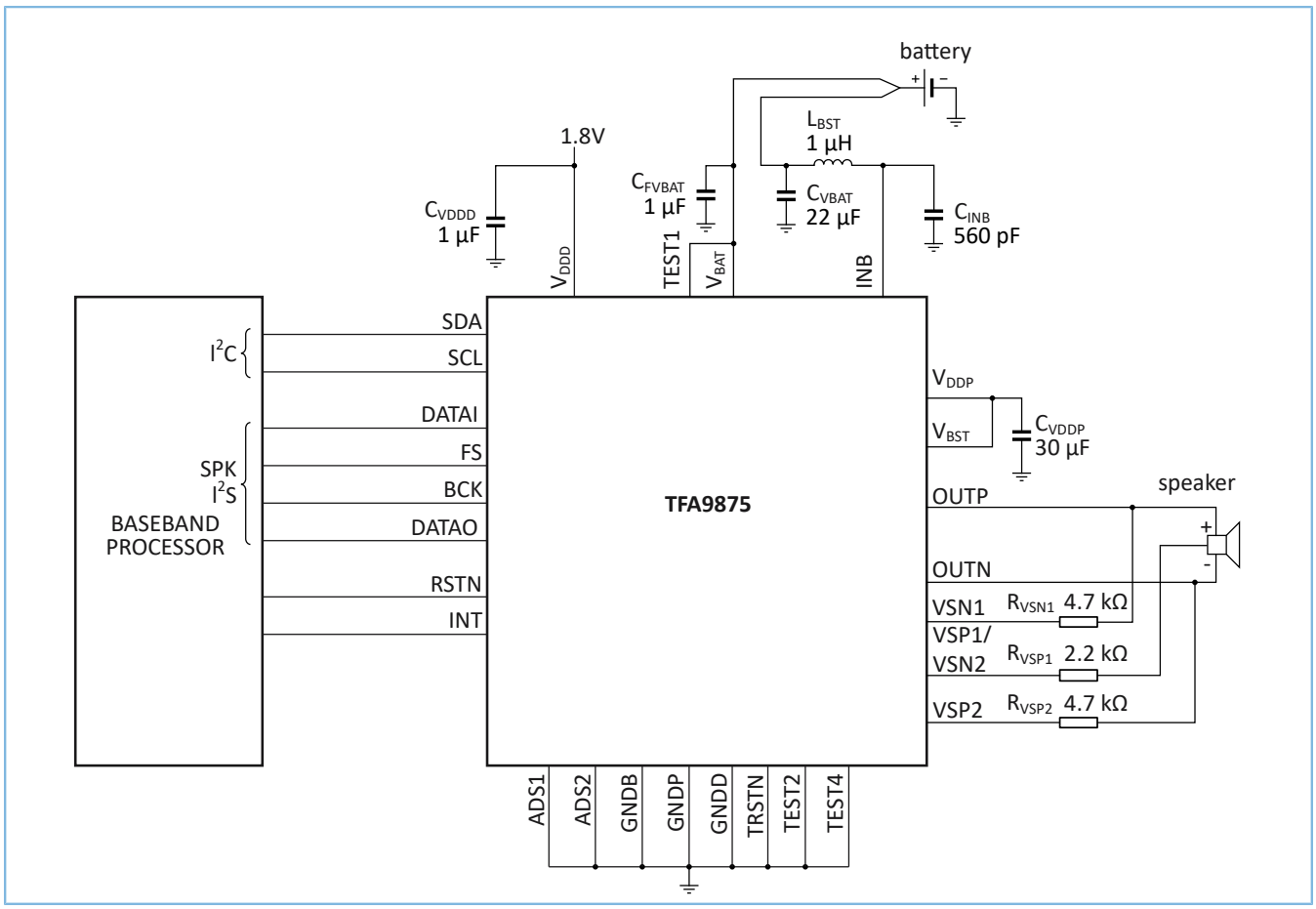


Figure 12-1: Typical mono application dual voltage sense

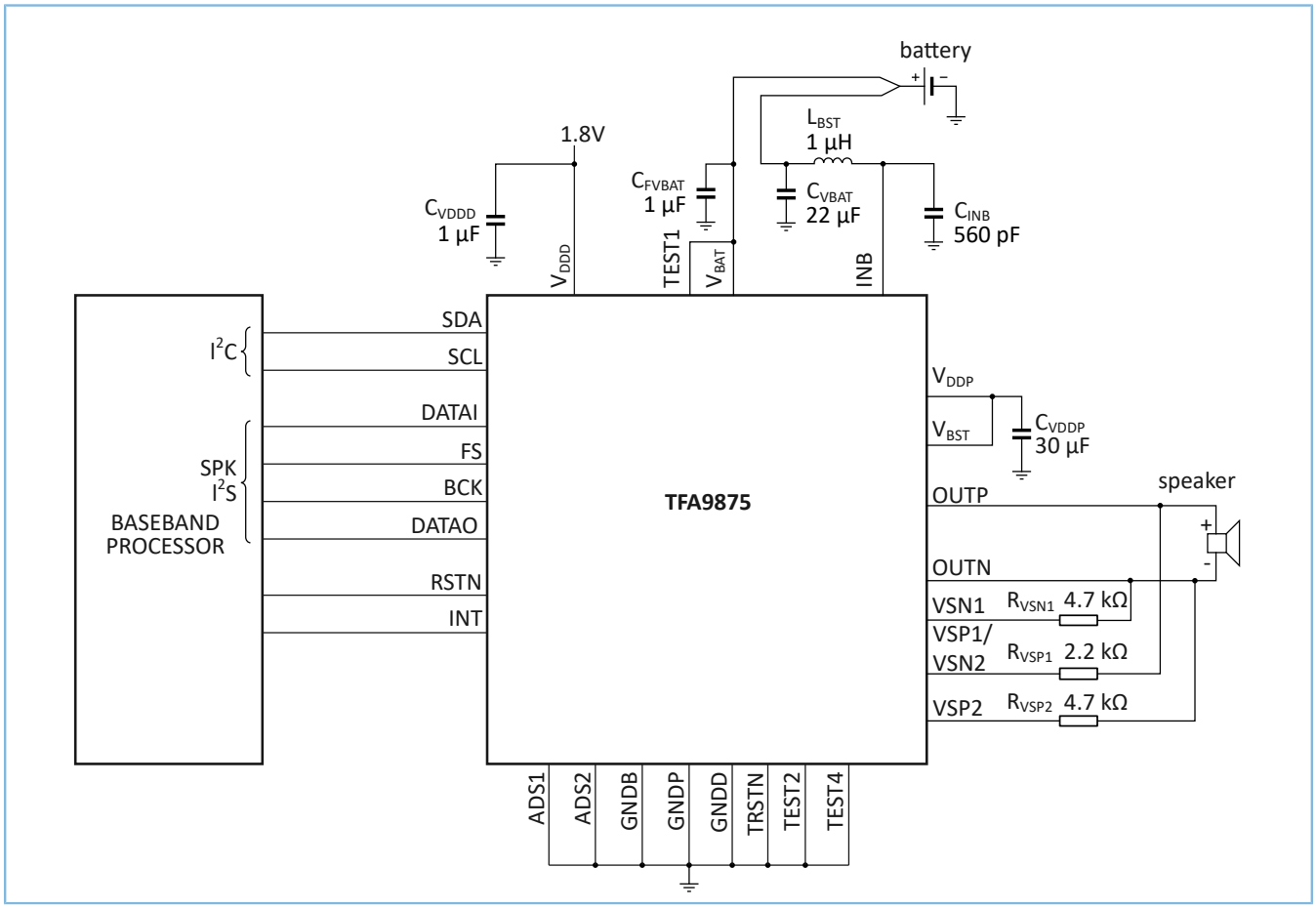


Figure 12-2: Typical mono application single voltage sense

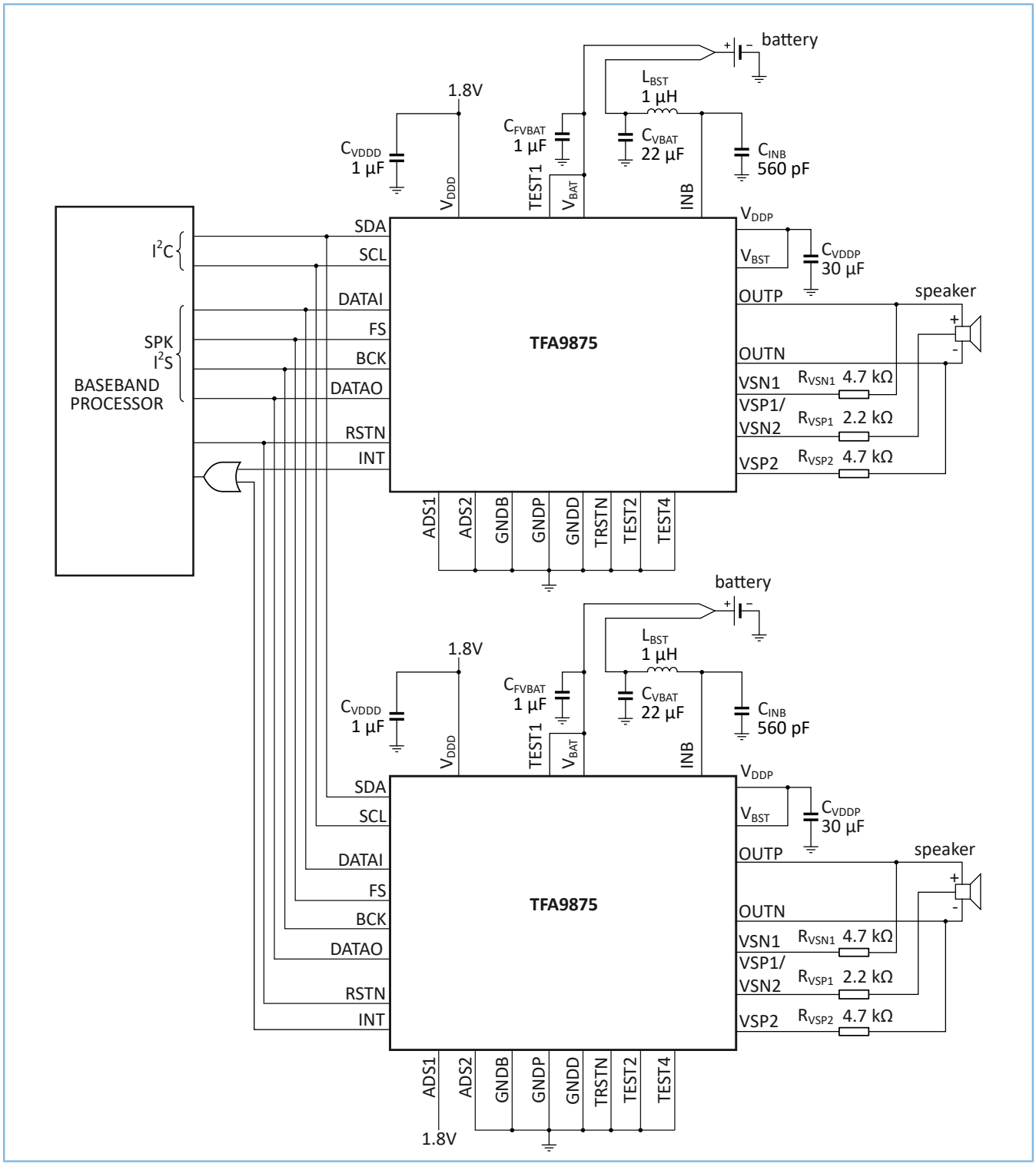


Figure 12-3: Typical stereo application dual voltage sense

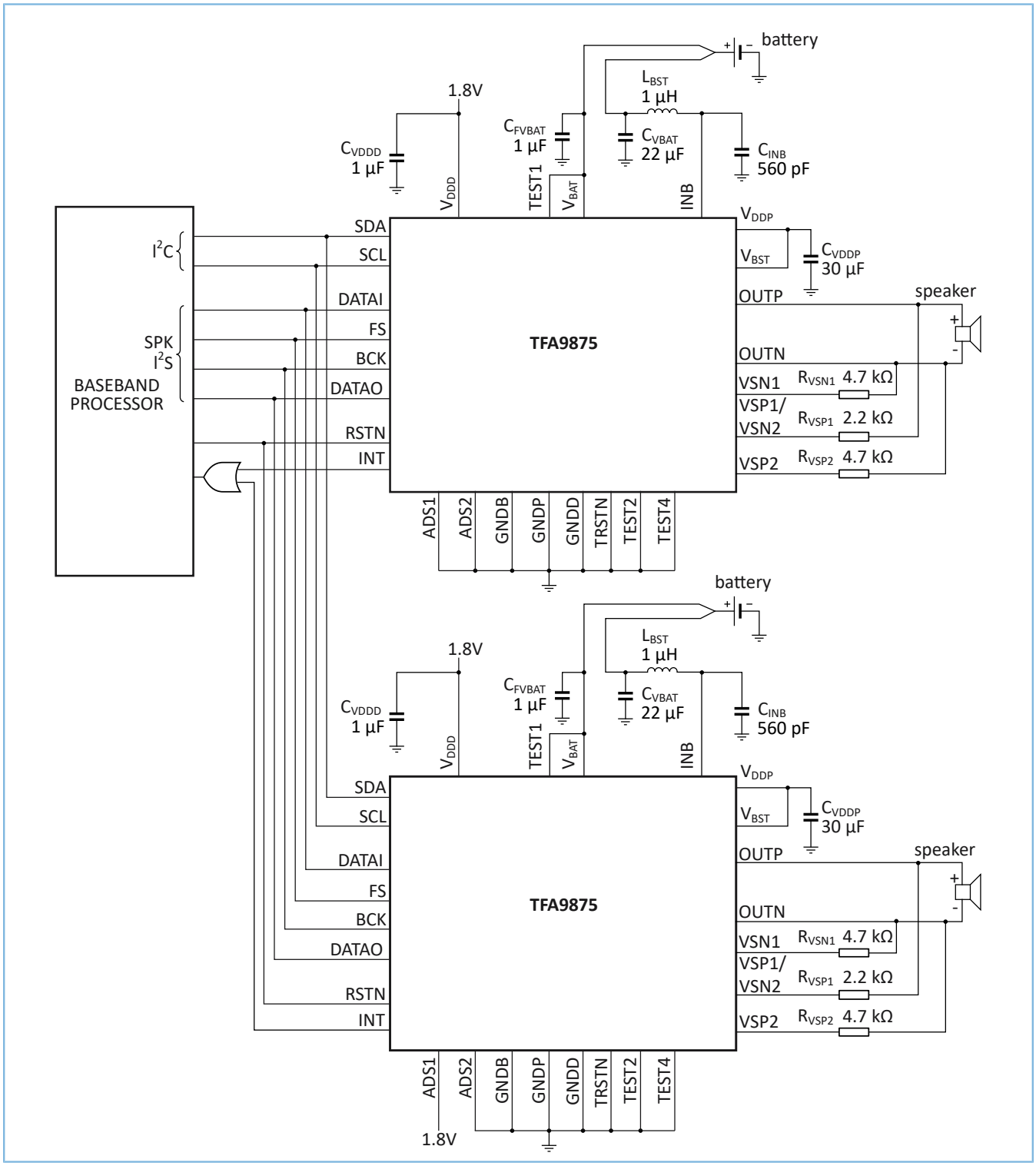
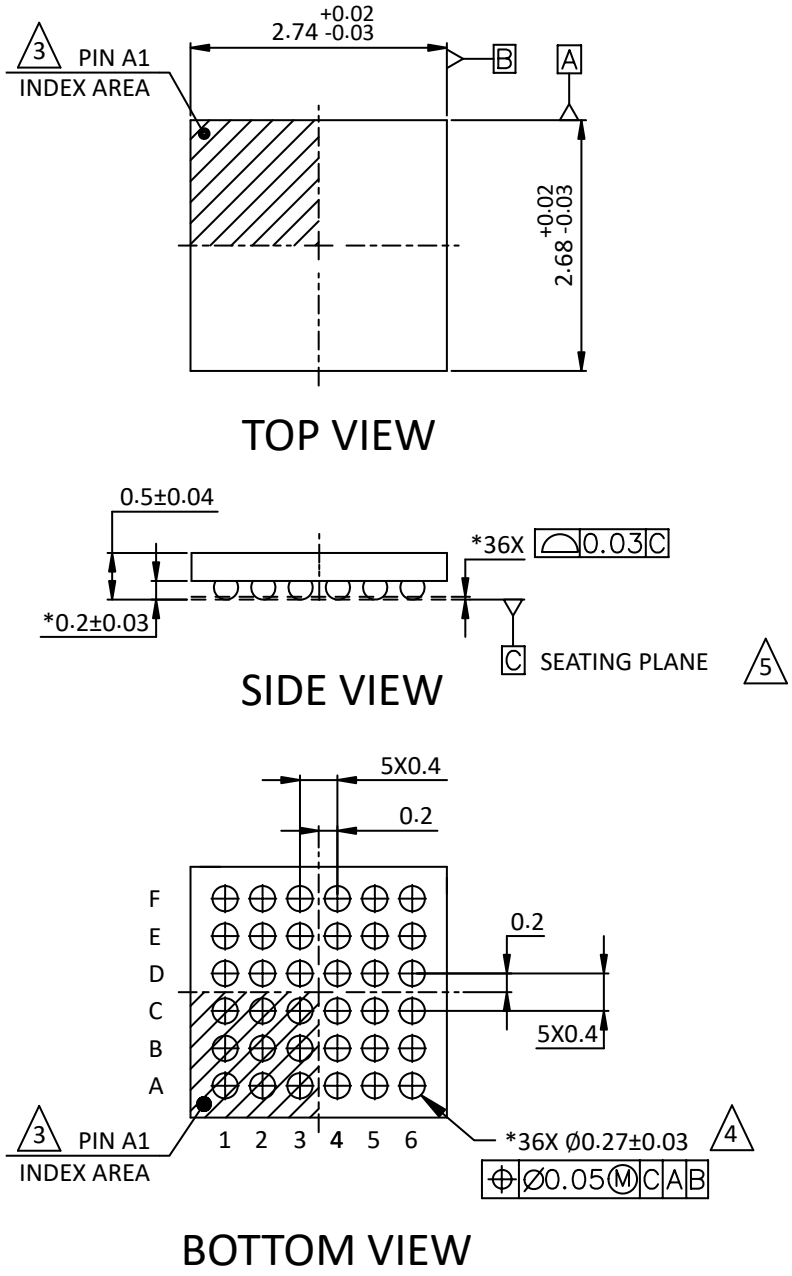


Figure 12-4: Typical stereo application single voltage sense

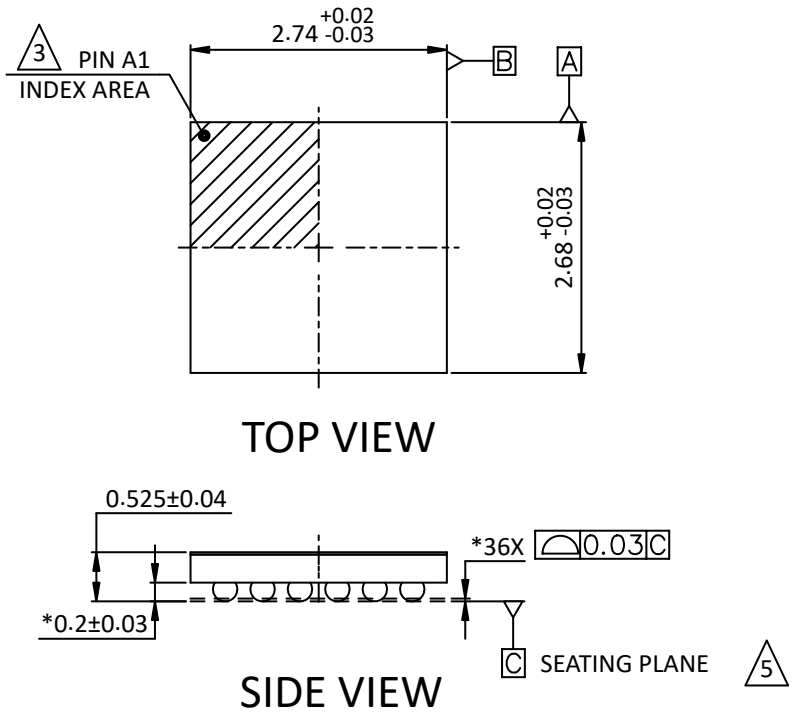
13 Package outline



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. "*"IS KEY CONTROL DIMENSION.

Figure 13-1: Package outline WLCSP36; no back side coating



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.
7. "*"IS KEY CONTROL DIMENSION.

Figure 13-2: Package outline WLCSP36; with back side coating

14 Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 14-1) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14-1.

Table 14-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 14-1.

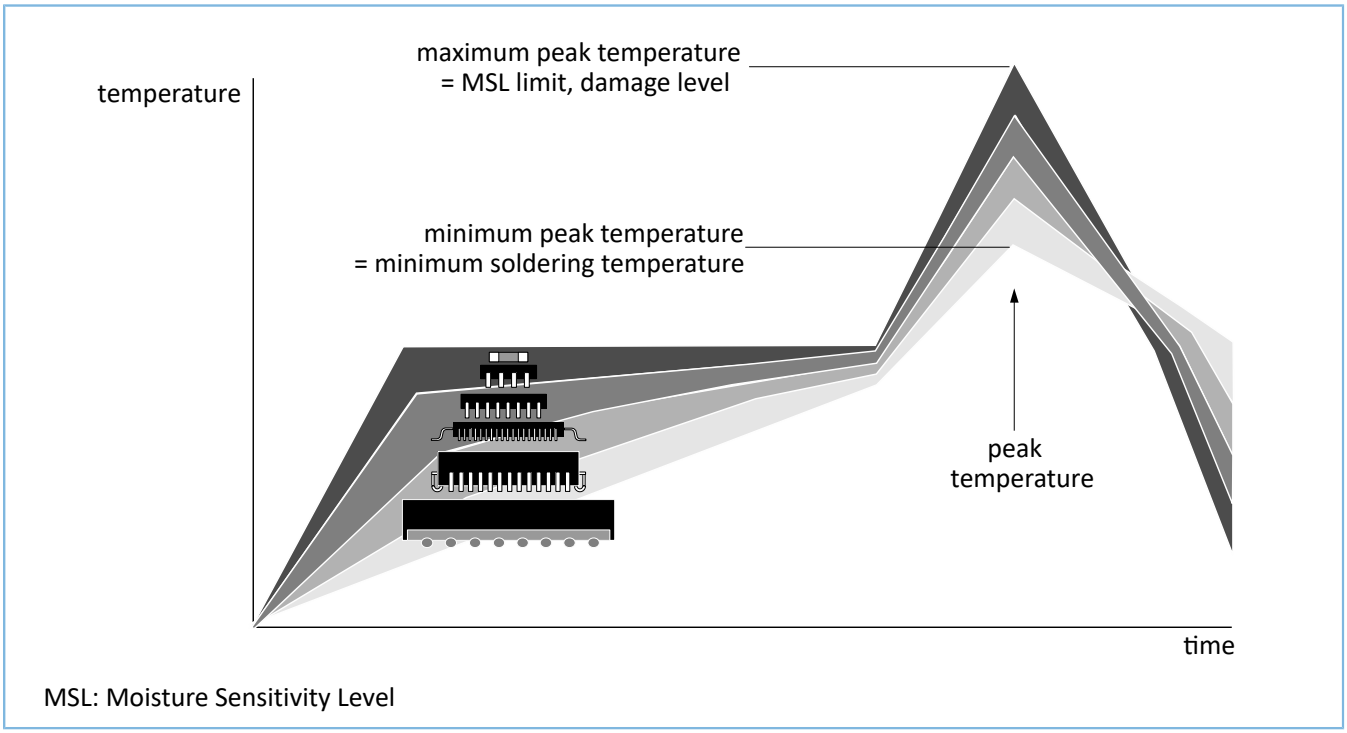


Figure 14-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15 Legal and Contact Information

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16 Revision history

Table 16-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9875_SDS - Rev 1.0	20211117	released data sheet	-	
modifications:	-			