TFA9878_SDS

High Efficiency Class-D Audio Amplifier

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Contents

1 General description

The TFA9878 is a high efficiency 10.0 V boosted class-D audio amplifier. It can deliver up to 10.0 W peak output power into an 8 Ω speaker and up to 11.8 W peak output power into a 6 Ω speaker, at a supply voltage of 4.0 V. The internal adaptive DC-to-DC converter raises the supply voltage up to 10.0 V, providing ample headroom for major improvements in sound quality.

Internal adaptive DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary, maximizing the output power of the class-D audio amplifier while limiting quiescent power consumption.

The device can be configured to drive either a hands-free speaker (4 Ω to 8 Ω) for audio playback or a receiver speaker (32 Ω), for handset playback. So, it can be embedded in platforms supporting both a hands-free speaker and a handset speaker. The maximum output power and the noise levels are lower in handset call use case than in hands-free call use case.

The TFA9878 also incorporates battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which could cause a system under voltage. This circuitry minimizes the impact of a falling battery voltage by preventing unexpected device switch off due to excessive current drawn from the battery.

The device contains MIPI v 1.1 compliant SoundWire interface which is used for audio data and control communication with the audio host. Furthermore, it can be used in legacy mode where TDM is used as audio interface and I^2C used for controlling the device.

The TFA9878 is available in a 36-bump wafer level chip-size package (WLCSP) with a 400 µm pitch.

2 Features and benefits

- High output power: 5.6 W (average) into 8 Ω at 4.0 V supply voltage (THD = 1 %)
- Supports handset and hands-free speaker configurations
- Ultra-low noise 7 µV mode in handset call with moderate output power
- High efficiency, low power dissipation speaker driver
- Low battery consumption < 125 mA (P_o = 380 mW, average music power)
- Adaptive DC-to-DC converter increases the supply voltage smoothly when switching between fixed boost and adaptive boost modes, preventing that large battery supply spikes and limiting quiescent power consumption occur.
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- SoundWire v 1.1 MIPI-compliant interface for audio and control
- Legacy I^2C-bus control interface (400 kHz)
- Legacy TDM audio interface
- Low latency 64 fs, 128 fs PDM via SoundWire
- Speaker current and voltage monitoring for acoustic echo cancellation (AEC) at the host
- 16 kHz/32 kHz/44.1 kHz/48 kHz sample frequencies supported
- Ultrasonic support with sample frequency of 96 kHz
- Programmable interrupt control via a dedicated interrupt pin
- Low RF susceptibility
- Overtemperature protection
- 15 kV system-level ESD protection without external components on amplifier output

3 Quick reference data

Table 3-1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD} in application	2.7	-	5.5	V
V_{DDD}	digital supply voltage	on pin VDDD	1.65	1.8	1.95	V
V_{DDP}	power supply voltage	on pin VDDP	2.7	-	10.2	V
I_{BAT}	battery supply current on VBAT pin	normal power mode; operating mode with load R_L = 6 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW, (average music power), V_{BAT} = 4.0 V; V_{BST} = 10 V	-	125	-	mA
		low-power mode, amplifier switching; input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V	-	5.5	-	mA
		idle power mode; amplifier ready to receive signal; input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V	-	0.2	-	mA
		power-down state	-	1	-	µA
I_{DDD}	digital supply current on VDDD pin	normal power mode; operating mode with load R_L = 6 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW, (average music power); V_{BAT} = 4.0 V; V_{BST} = 10 V	-	6.5	-	mA
		low-power mode; amplifier switching; input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V	-	5	-	mA
		idle power mode; amplifier ready to receive signal; active signal level detection; P_o = 0 mW; V_{BAT} = 4.0 V	-	2.9	-	mA
		power-down state	1.6	3	30	µA
R_L	load resistance		3.2	-	38	Ω
$P_{i(AV)}$	average input power	normal power mode; P_o = 0 mW	-	40	-	mW

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		low-power mode; P_o = 0 mW	-	25	-	mW
		idle power mode; P_o = 0 mW	-	5	-	mW
$P_{o(AV)}$	average output power	THD+N = 1 %; (R_L = 8 Ω; L_L = 44 µH); V_{BST} = 10.0 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V	5.3	5.6	-	W
		THD+N = 1 %; (R_L = 6 Ω; L_L = 32 µH); V_{BST} = 10.0 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V	5.8	6.1	-	W
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; low-noise mode; f_s = 48 kHz	-	7	-	µV

4 Applications

- Mobile phones and tablets
- Portable navigation devices (PND)
- Notebooks/netbooks

5 Ordering information

Table 5-1: Ordering information

Type number	Package		
	Name	Description	Version
TFA9878UK/N1	WLCSP36	wafer level chip-scale package; 36 bumps; 0.4 mm pitch,	SOT1780-10
TFA9878BUK/N1	WLCSP36	wafer level chip-scale package; 36 bumps; 0.4 mm pitch, back side coating	SOT1780-9

6 Block diagram

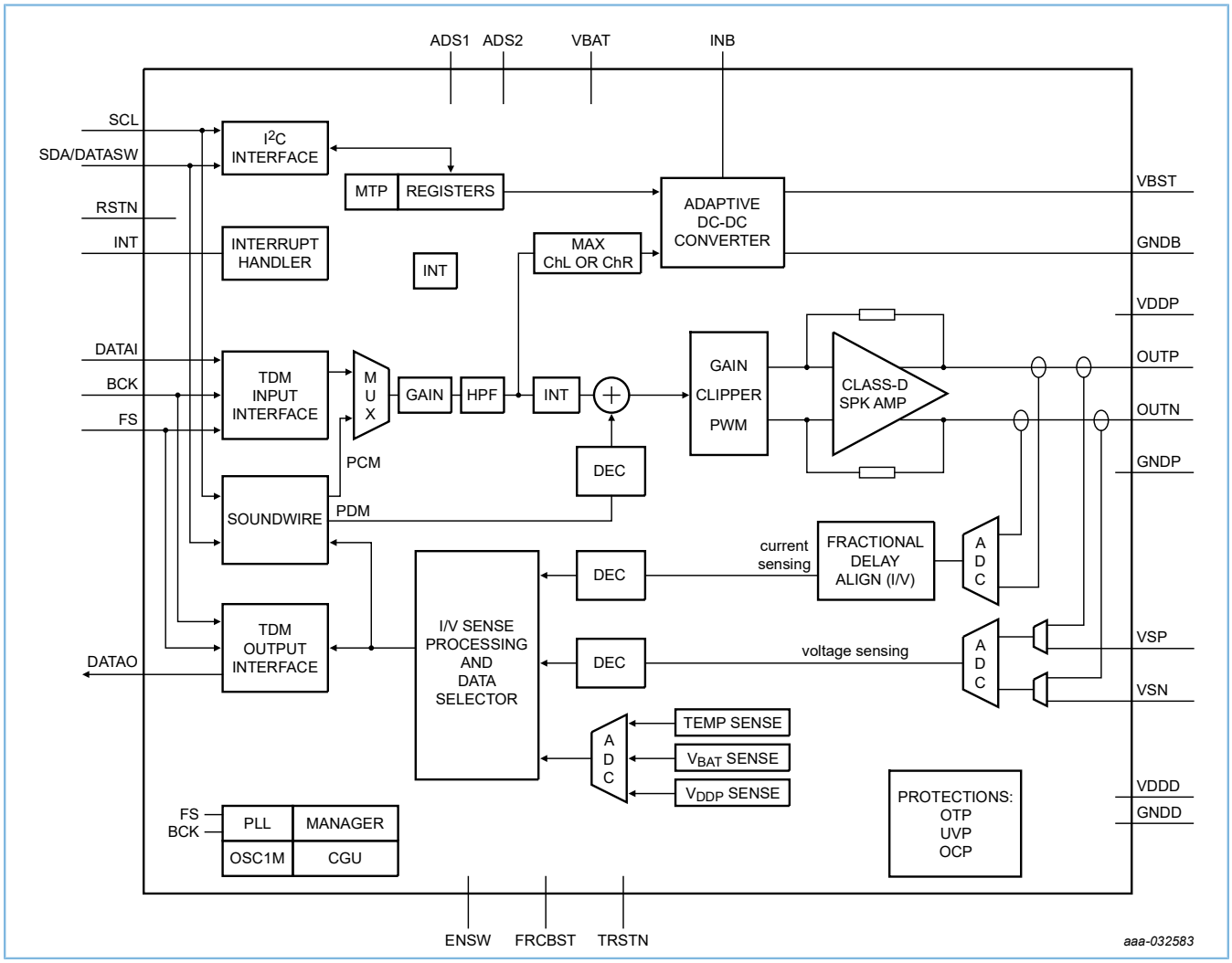
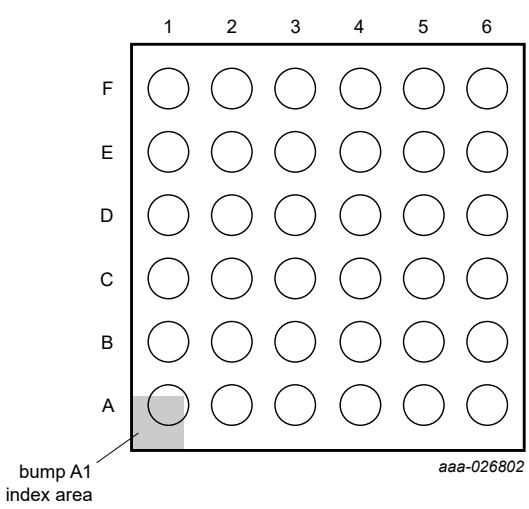


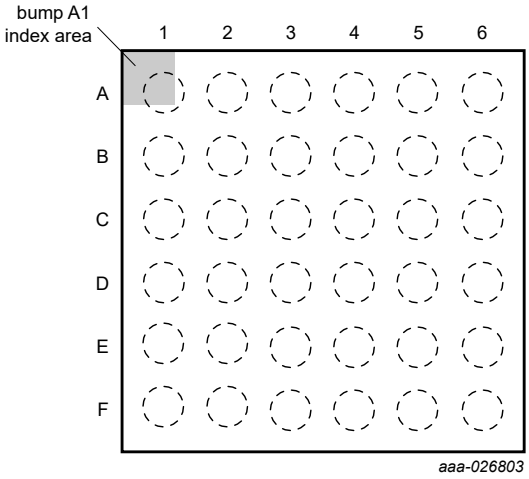
Figure 6-1: Block diagram

7 Pinning information

7.1 Pinning



a. Bottom View



b. Transparent top view

Figure 7-1: Bump configuration

	1	2	3	4	5	6
A	DATAI	DATAO	VDDD	GNDD	VBAT	SDA/DATASW
B	FS	ADS1	RSTN	ADS2	INT	SCL/CLKSW
C	BCK	TRSTN	VSP	FRCBST	ENSW	VSN
D	GNDB	GNDB	GNDB	GNDD	GNDP	GNDD
E	INB	INB	INB	OUTP	GNDP	OUTN
F	VBST	VBST	VBST	VDDP	VDDP	VDDP

aaa-032584

Transparent top view

Figure 7-2: Bump mapping

Table 7-1: Pinning

Symbol	Pin	Type	Description
DATAI	A1	I	digital audio data input for TDM interface
DATAO	A2	O	digital audio data output for TDM interface
VDDD	A3	P	digital supply voltage
GNDD	A4	P	digital ground

Symbol	Pin	Type	Description
VBAT	A5	P	battery supply voltage
SDA/DATASW	A6	I/O	I^2C-bus or Soundwire data input/output depending on ENSW
FS	B1	I	digital audio frame sync input for TDM interface
ADS1	B2	I	digital address select input 1
RSTN	B3	I	active low reset input
ADS2	B4	I	digital address select input 2
INT	B5	O	digital interrupt output
SCL/CLKSW	B6	I/O	I^2C-bus or SoundWire clock input/output depending on ENSW
BCK	C1	I	digital audio bit clock input for TDM interface
TRSTN	C2	I	test signal input TRSTN, connect to PCB ground
VSP	C3	I/O	voltage sense positive input
FRCBST	C4	I/O	force boost
ENSW	C5	I/O	enable SoundWire interface.
VSN	C6	I/O	voltage sense negative
GNDB	D1	P	booster ground
GNDB	D2	P	booster ground
GNDB	D3	P	booster ground
GNDD	D4	P	digital ground
GNDP	D5	P	power ground
GNDD	D6	P	digital ground
INB	E1	P	DC-to-DC boost converter input
INB	E2	P	DC-to-DC boost converter input
INB	E3	P	DC-to-DC boost converter input
OUTP	E4	O	non-inverting output
GNDP	E5	P	power ground
OUTN	E6	O	inverting output
VBST	F1	O	boosted supply voltage output
VBST	F2	O	boosted supply voltage output
VBST	F3	O	boosted supply voltage output

Symbol	Pin	Type	Description
VDDP	F4	P	power supply voltage
VDDP	F5	P	power supply voltage
VDDP	F6	P	power supply voltage

8 Functional description

The TFA9878 is a highly efficient bridge tied load (BTL) class-D audio amplifier as depicted in block diagram (see Figure 6-1).

TFA9878 contains a SoundWire interface v1.1 for audio and control. The 2-wire interface is multiplexed with I^2C pins.

Next to the legacy I^2C also legacy TDM audio interface is available for communicating with the audio host. It also offers the possibility of providing an ultrasonic path to the speaker.

At low battery voltage levels, the gain is automatically reduced to limit battery current (when battery safeguard is enabled).

The digital audio stream is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filter less speaker drive.

An adaptive DC-to-DC converter boosts the output voltage to the level that the class-D amplifier requires.

9 Limiting values

Table 9-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT		−0.3	+6	V
V_{BST}	booster output voltage	on pin VBST	[1]	−0.3	+12	V
V_{INB}	booster input voltage	on pin INB	[1]	−0.3	+12	V
V_{DDP}	power supply voltage	on pin VDDP	[1]	−0.3	+12	V
V_O	output voltage	on speaker connections; pins OUTP and OUTN	[1]	−0.3	+12	V
V_{sense}	sense voltage	sense input voltage on pins VSN and VSP	[1]	−0.3	+12	V
V_{DDD}	digital supply voltage	on pin VDDD		−0.3	+2.5	V
V_{low}	low voltage	on pins ENSW/FRCBST		−0.3	+2.5	V
T_j	junction temperature			-	125	°C
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to human body model (HBM)		−2	+2	kV
		according to charge device model (CDM)		−500	+500	V

[1] Using the Goodix Technology demo board, with a 1 mm wire/PCB track length on INB pin, AC pulses between −6 V and +15 V can be observed without damaging the device. These spikes do not end up inside the actual device.

10 Thermal characteristics

Table 10-1: Primary states selection

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	30	K/W

11 Characteristics

11.1 DC characteristics

Table 11-1: DC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD} in application		2.7	-	5.5	V
V_{DDP}	power supply voltage	on pin VDDP		2.7	-	10.2	V
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V
I_{BAT}	battery supply current	normal power mode; operating mode with load R_L = 6 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW, (average music power), V_{BAT} = 4.0 V; V_{BST} = 10 V		-	125	-	mA
		low-power mode, amplifier switching; input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V		-	5.5	-	mA
		idle power mode; amplifier ready to receive signal; input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V		-	0.2	-	mA
		power-down state	[2]	-	1	-	µA
I_{DDD}	digital supply current on VDDD pin	normal power mode; operating mode with load R_L = 6 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW, (average music power); V_{BAT} = 4.0 V; V_{BST} = 10 V		-	6.5	-	mA
		low-power mode; amplifier switching; input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V		-	5	-	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		idle power mode; amplifier ready to receive signal; active signal level detection; P_o = 0 mW; V_{BAT} = 4.0 V		-	2.9	-	mA
		power-down state		1.6	3	30	µA
Pins FS, BCK, DATAI, ADS1, ADS2, SCL/SCLSW, SDA/DATASW, RSTN, FRCBST, ENSW							
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDD}$	V
R_{pu}	pull-up resistance	pin RSTN		-	20	-	kΩ
C_{in}	input capacitance	pins FS, BCK, DATAI, ADS1, ADS2, RSTN, and FRCBST	[3]	-	-	5	pF
		pins SCL/SCLSW and SDA/DATASW	[3]	-	-	10	pF
I_{LI}	input leakage current	1.8 V on pins FS, BCK, DATAI, ADS1, ADS2, and FRCBST		-	-	0.1	µA
		1.8 V on pins SCL/SCLSW and SDA/DATASW		-	-	0.5	µA
Pins DATAO, INT, push-pull output stages							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DDD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins SDA, open-drain outputs, external resistor to V_{DDD}							
V_{OH}	HIGH-level output voltage			V_{DDD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA		-	-	400	mV
Pins OUTP, OUTN							
R_{DSon}	drain-source on-state resistance	PMOS + NMOS transistors		-	430	520	mΩ
Protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	-	°C
$V_{ovp(VBAT)}$	overvoltage protection on pin VBAT			5.6	-	6.0	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{uvp(VBAT)}$	undervoltage protection on pin VBAT			2.3	-	2.7	V
$I_{O(ocp)}$	overcurrent protection output current			2.5	-	-	A
DC-to-DC converter							
V_{BST}	voltage on pin VBST	DCVOS = 111111; boost mode (after trim)	[4]	9.8	10	10.2	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] As long as RSTN is LOW, a current of maximum 4 mA can be drawn from the battery.
[3] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.
[4] Boost switching frequency = 2 MHz in PWM mode.

11.2 AC characteristics

Table 11-2: AC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(AV)}$	average output power	hands-free speaker; THD+N = 1 %; V_{DDD} = 1.8 V					
		R_L = 8 Ω; L_L = 44 µH; f_s = 48 kHz; V_{BST} = 10.0 V; V_{BAT} = 4.0 V		5.3	5.6	-	W
		R_L = 6 Ω; L_L = 32 µH); f_s = 48 kHz; V_{BST} = 10.0 V; V_{BAT} = 4.0 V		5.8	6.1	-	W
		R_L = 4 Ω; L_L = 22 µH); f_s = 48 kHz; V_{BST} = 9.0 V; V_{BAT} = 4.0 V		6	6.2	-	W
		receiver speaker; THD+N = 1 %; V_{BST} = 10.0 V					
		R_L = 32 Ω; voice mode		-	0.2	-	W
		R_L = 32 Ω; audio mode		-	1.5	-	W
Amplifier output pins (OUTP and OUTN)							
$\lvert V_{O(offset)} \rvert$	output offset voltage	DC-to-DC in follower mode		-	-	0.5	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier performances							
η_{po}	output power efficiency	on pin VBAT; operating mode with load R_L = 6 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW (average music power); V_{BAT} = 4.0 V	[2]	-	76	-	%
		on pin VBAT; input: 100 Hz sine wave; R_L = 8 Ω; DC-to-DC in tracking boost mode; V_{BAT} = 4.0 V; P_o = 600 mW	[2]	-	88	-	%
		on pin V_{BAT}; input: 100 Hz sine wave; R_L = 8 Ω; DC-to-DC in tracking boost mode; V_{BAT} = 4.0 V; P_o = 4 W	[2]	-	82	-	%
THD+N	total harmonic distortion-plus-noise	V_{DDP} > 9 V; P_o = 2.0 W; R_L = 8 Ω	[3]	-	-	0.05	%
		V_{DDP} > 9 V; P_o = 2.0 W; R_L = 4 Ω	[3]	-	-	0.09	%
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; normal mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, or 96 kHz	[2]	-	25	-	μV
		a-weighted; no input signal; low-noise mode; low-power mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, or 96 kHz	[2]	-	7	-	μV
		a-weighted; no input signal; idle power mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, or 96 kHz	[2]	-	1	-	μV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %); output noise voltage ($V_{n(o)}$); no signal applied; low-noise mode	[2]	114	120	-	dB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S/N	signal-to-noise ratio	a-weighted; V_{BAT} = 3.4 V to 5 V; maximum signal at THD = 1 %	[2]	-	100	-	dB
PSRR	power supply rejection ratio	from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}) f_{ripple} = 217 Hz square wave; V_{ripple} = 50 $mV_{(p-p)}$; P_o = 0; idle-power mode on; low-noise mode on		95	105	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 20 Hz to 1 kHz sine wave; V_{ripple} = 200 mV (RMS); P_o = 0; low-power mode on; low-noise mode on		60	80	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 1 kHz to 20 kHz sine wave; V_{ripple} = 200 mV (RMS); P_o = 0; low-power mode on; low-noise mode on		55	60	-	dB
ΔG/Δf	gain variation with frequency	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V		−0.1	-	+0.7	dB
V_{POP}	pop noise voltage	P_o = 0; DC-to-DC in follower mode		-	-	1	mV
R_L	load resistance			3.2	8	38	Ω
C_L	load capacitance			-	-	200	pF
f_{sw}	switching frequency	f_s = 16 kHz, 32 kHz, 48 kHz, or 96 kHz		-	768	-	kHz
		f_s = 44.1 kHz		-	705.6	-	kHz
$G_{(TDM-VO)}$	TDM to V_O gain	INPLEV = 0 dB		6	-	21	dB
Amplifier power-up, power-down, and propagation delays							
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK; f_s = 48 kHz		-	2	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time	f_s = 48 kHz		-	1	-	ms

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time			-	32	-	µs
$t_{d(alarm)}$	alarm delay time			-	200	-	ms
t_{PD}	propagation delay	delta propagation delay between left and right in stereo application = 0.1 FS					
		f_s = 16 kHz		-	940	950	µs
		f_s = 32 kHz		-	720	750	µs
		f_s = 44.1 kHz		-	660	700	µs
		f_s = 48 kHz		-	650	700	µs
		f_s = 96 kHz		-	-	580	µs
Booster inductance							
L_{bst}	boost inductance			0.33	1.0	2.2	µH
Voltage sensing and current sensing performance							
S/N	signal-to-noise ratio	I_O = 1.1 A (peak); a-weighted		62	65	-	dB
$\Delta V_{sense}/I_{sense}$	V_{sense}/I_{sense} ratio mismatch	pilot tone: −40 dBFS	[4]	-	2	-	%
THD+N	total harmonic distortion-plus-noise	f_i = 20 Hz to 20 kHz; V_i = −12 dBFS		-	-	0.75	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.
[3] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance (speaker).
[4] Intended for Speaker protection. In combination with Goodix Speaker protection, a speaker temperature accuracy of ± 10 °C can be realized.

11.3 TDM timing characteristics

Table 11-3: TDM bus interface characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin FS; audio mode	[2]	16	-	48	kHz
		on pin FS; ultrasonic mode		-	-	96	kHz
f_{clk}	clock frequency	on pin BCK; audio mode	[2]	$32f_s$	-	$384f_s$	kHz
		on pin BCK; ultrasonic mode		-	-	$96f_s$	kHz
t_{su}	set-up time	FS edge to BCK HIGH	[3]	10	-	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to FS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns
t_J	external clock jitter	PLL locked on FS	[4]	-	-	20	ns
		PLL locked on BCK	[4]	-	-	2	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. The BCK and WS signals must be present for the clock to operate correctly.
[3] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.
[4] When the PLL is locked on FS, the system is less sensitive to jitter, and noise performance can be guaranteed.

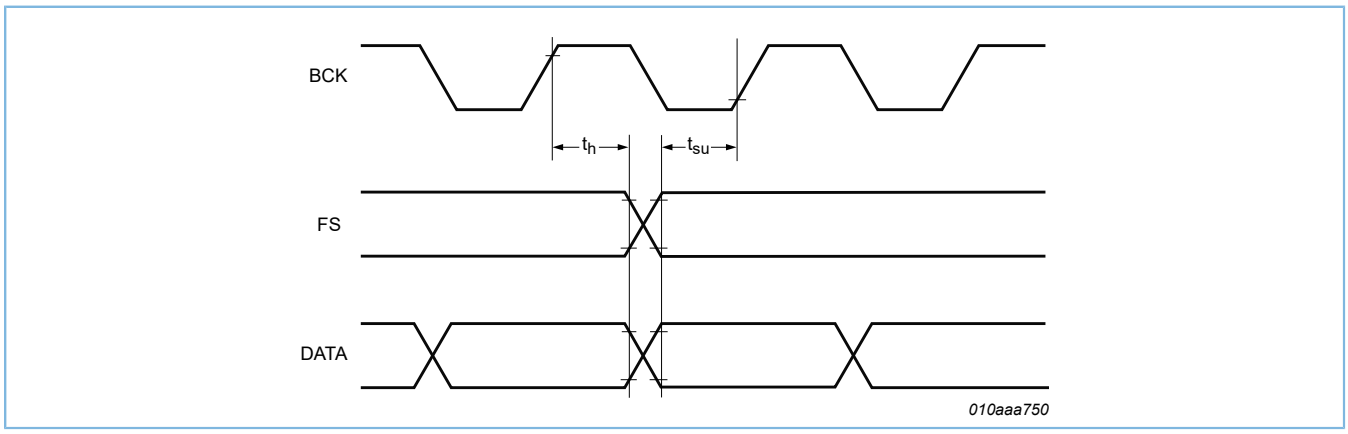


Figure 11-1: TDM timing

11.4 I^2C timing characteristics

Table 11-4: I^2C-bus interface characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1C_b	-	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

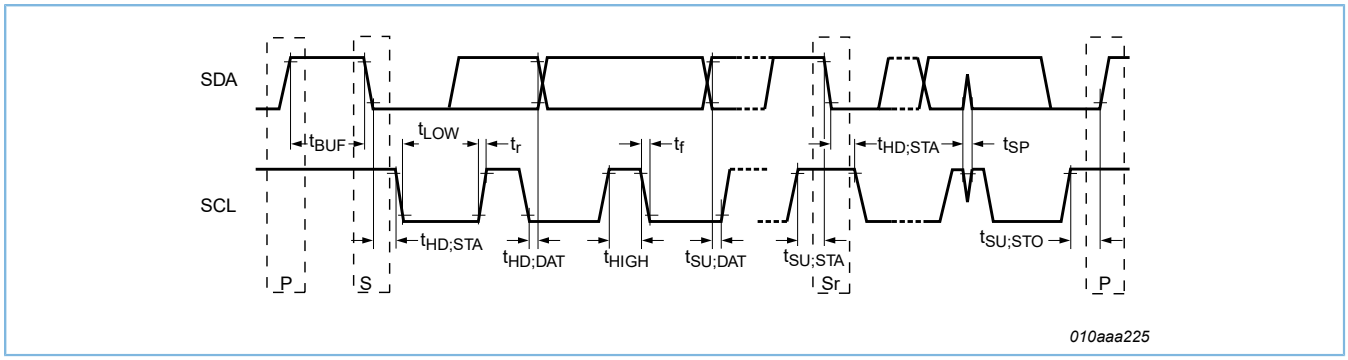


Figure 11-2: I²C timing

12 Application information

12.1 Application diagrams

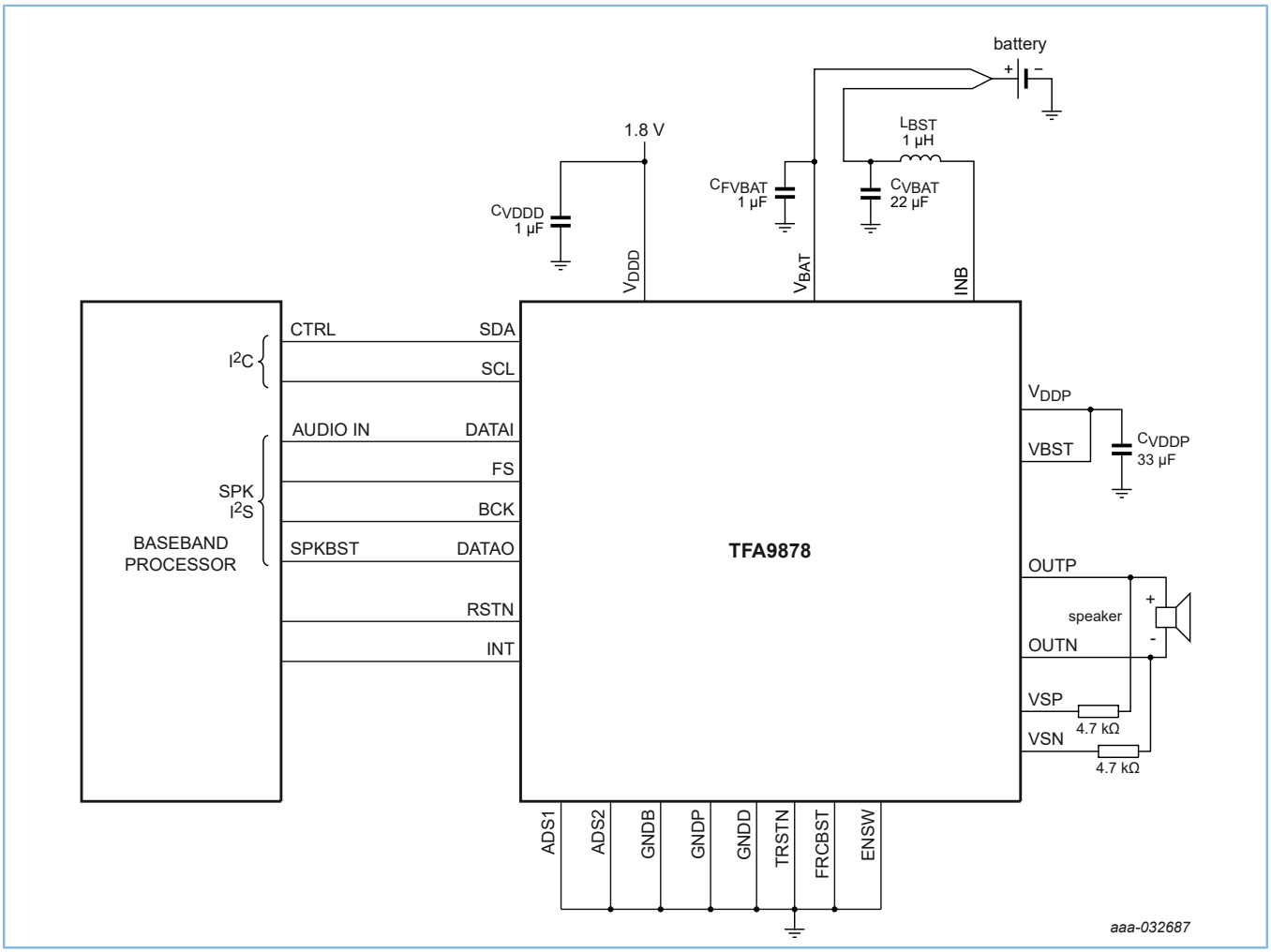


Figure 12-1: Typical mono application

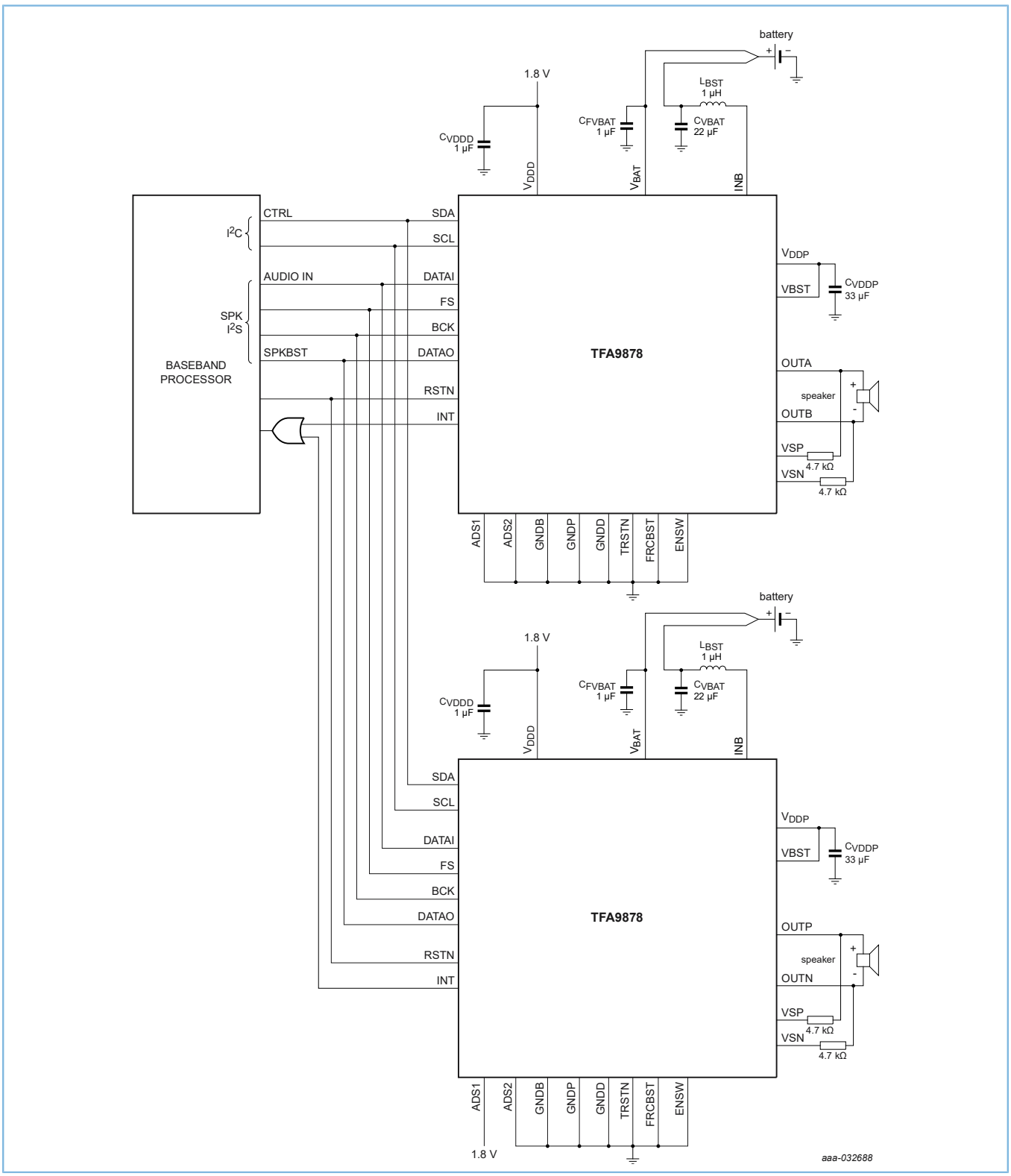


Figure 12-2: Typical stereo application

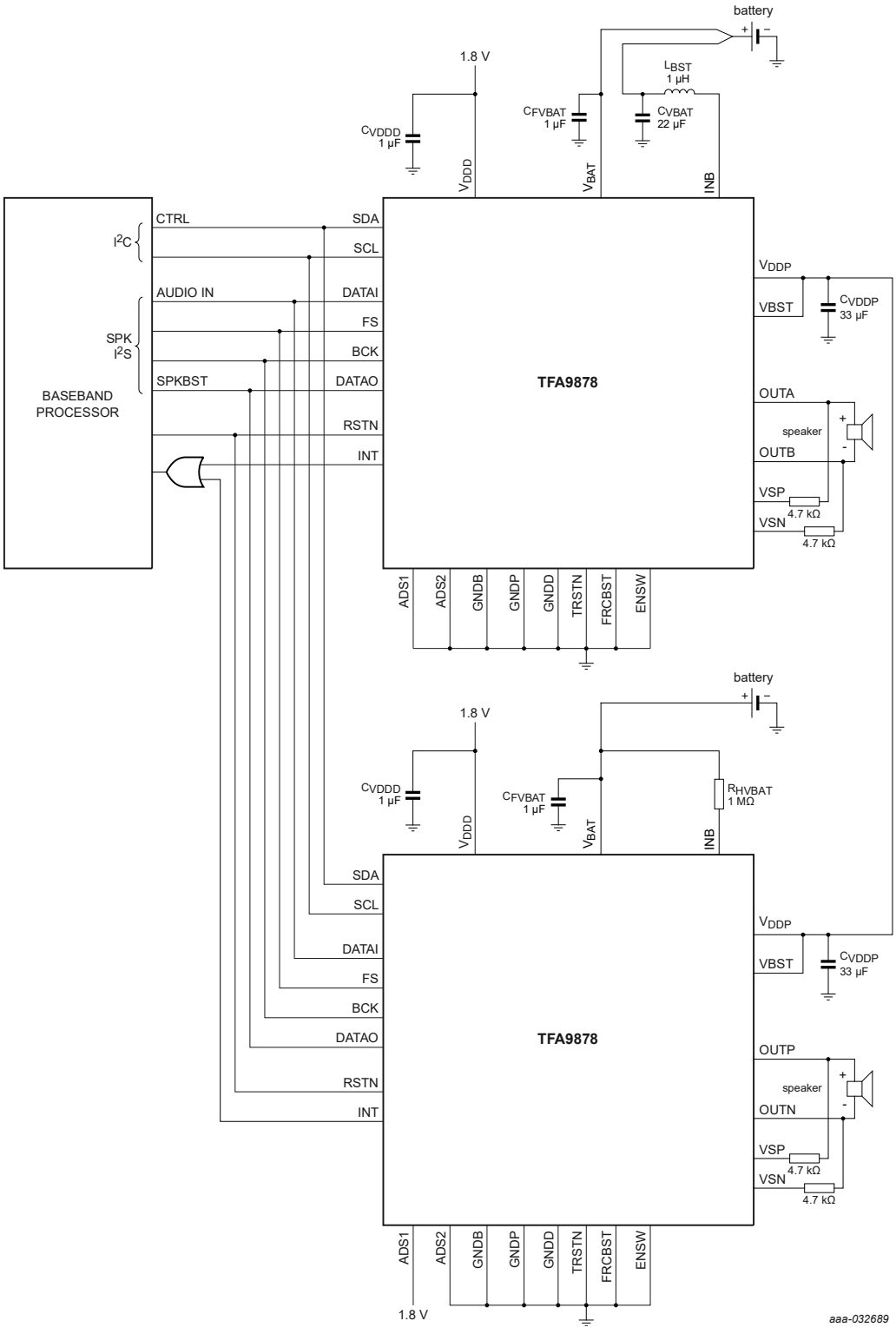


Figure 12-3: Typical stereo application shared booster

13 Package outline

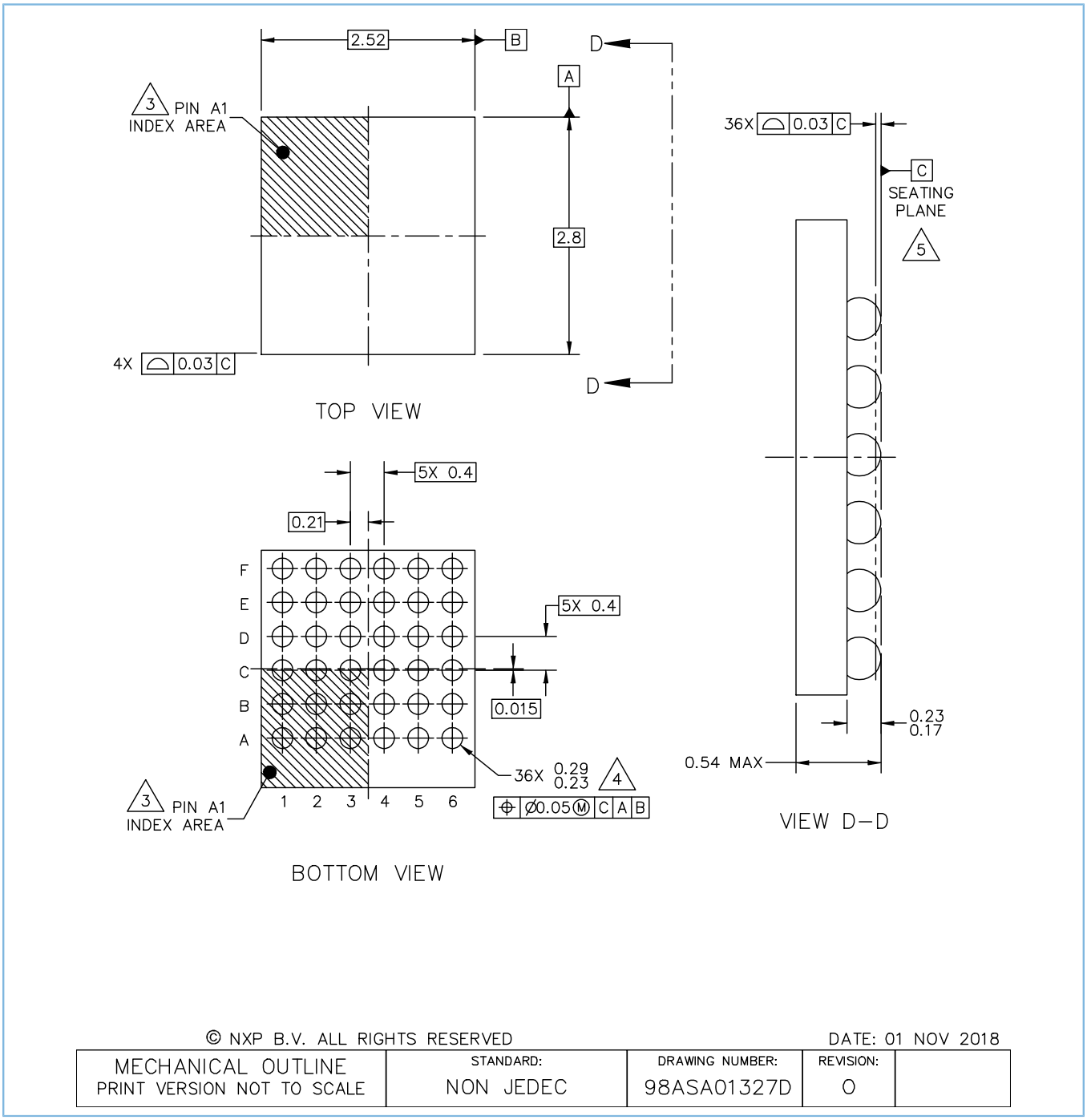


Figure 13-1: Package outline WLCSP36 (SOT1780-10); no back side coating

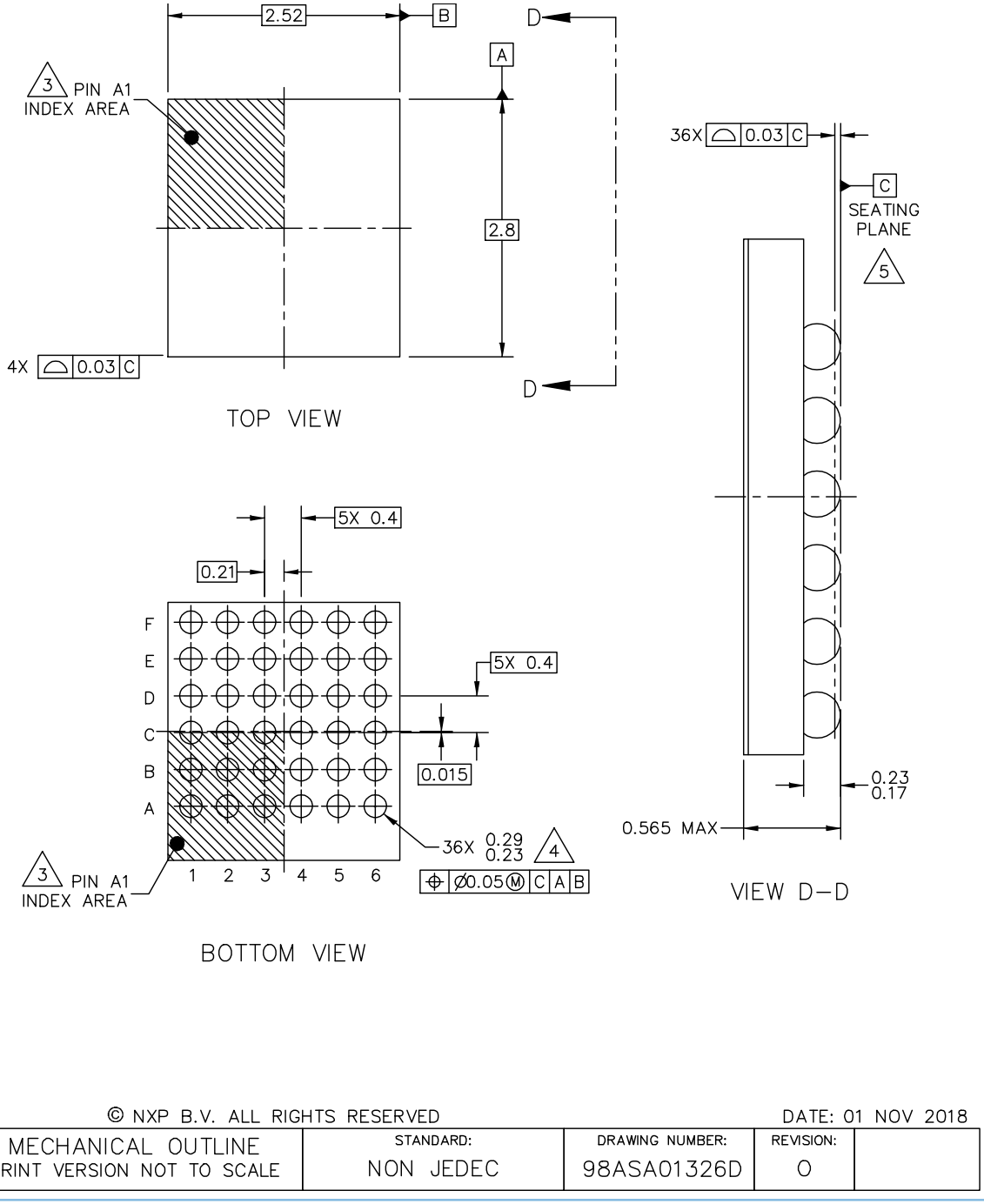


Figure 13-2: Package outline WLCSP36 (SOT1780-9); with back side coating

14 Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix Technology WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

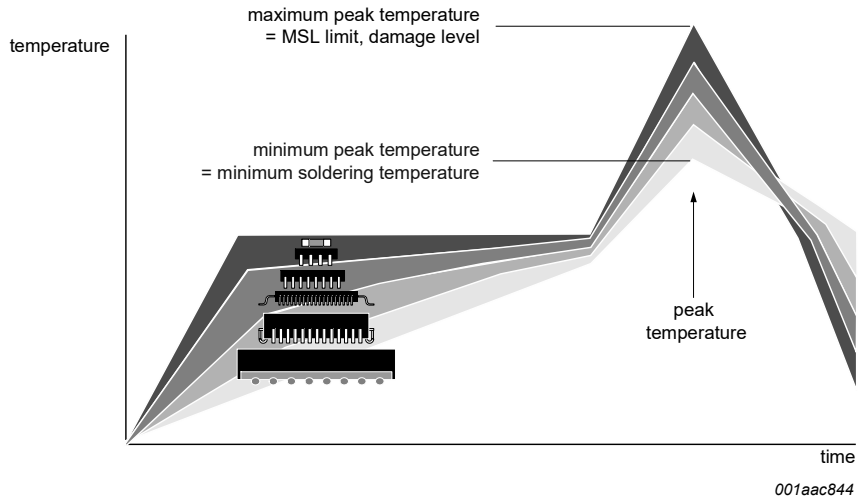
- Lead-free versus SnPb soldering: A lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 14-1) than a SnPb process, therefore reducing the process window.
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board.
- Reflow temperature profile: This profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. The peak temperature must be high enough for the solder to make reliable solder joints (a solder paste characteristic) and low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14-1.

Table 14-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must always be respected.

Studies have shown that small packages reach higher temperatures during reflow soldering (see Figure 14-1).



MSL: Moisture Sensitivity Level

Figure 14-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to thermal expansion coefficient (TEC) differences between substrate and chip.

14.3.2 Quality of solder joint

When the solder from the bump has wetted the entire solder land, a flip-chip joint is considered to be a good joint. The surface of the joint must be smooth and the shape symmetrical. The soldered joints on a chip must be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, that is, low bumps with large diameter. No failures have been found that are related to these voids. To monitor defects such as bridging, open circuits, and voids, solder joint inspection after reflow can be done with X-ray.

14.3.3 Rework

In general, rework is not recommended. By rework, we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip are damaged. In that case, do not reuse the chip.

When the substrate is heated until it is certain that all solder joints are molten, the device can be removed. The chip can then be removed carefully from the substrate without damaging the tracks and solder lands on the substrate. Use plastic tweezers to remove the device, because metal tweezers can damage the silicon. The surface of the substrate must be cleaned carefully and all solder and flux residue and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side and on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15 Legal and contact information

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16 Revision history

Table 16-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9878_SDS v 3.0	20200316	Product short data sheet	-	TFA9878_SDS v.2
Modifications:	• Updated document format based on Goodix template.			
TFA9878_SDS v.2	20191105	Product short data sheet	-	TFA9878_SDS v.1.1
Modifications:	• Text and graphic have been updated throughout this document.			
TFA9878_SDS v.1.1	20191014	Product short data sheet	-	TFA9878_SDS v.1
Modifications:	• External components "External components" has been updated. • Section 12.1 "Application diagrams": Added required values for voltage sense resistors and application diagrams updated accordingly.			
TFA9878_SDS v.1	20190923	Product short data sheet	-	-