



TFA9914_SDS

High Efficiency Class-D Amplifier for Haptic

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1 General description

The TFA9914 is a high efficiency 10 V boosted class-D haptic driver. It can deliver up to 5.6 W (AVG) output power into an 8 Ω load and up to 1.5 W (AVG) output power into 32 Ω load, at a battery supply voltage of 4.0 V. The internal adaptive DC-to-DC converter raises the power supply voltage up to 10 V, providing strong and sharp haptic feedbacks. Internal adaptive DC-to-DC conversion boosts the supply rail to provide additional headroom and output power. The supply voltage is only raised when necessary. It maximizes the output power of the class-D amplifier while limiting quiescent power consumption.

The device can be configured to drive from 8 Ω up to 32 Ω load, allowing it to be embedded in a wide variety of haptic platforms.

The TFA9914 also incorporates battery protection. By limiting the supply current when the battery voltage is low, it prevents the haptic system from drawing excessive load currents from the battery, which could cause a system undervoltage. This circuitry minimizes the impact of a falling battery voltage by preventing unexpected device switch off / shutdowns due to excessive current drawn from the battery.

The device features a second order closed loop architecture, used in a class-D amplifier, providing an excellent signal performance and high supply voltage ripple rejection. The data input interface is TDM and the control settings are communicated via an I²C-bus interface.

The TFA9914 is available in a 48-bump wafer level chip-size package (WLCSP) with a 400 μm pitch.

2 Features and benefits

- Fully integrated solution that includes class-D amplifier, DC-to-DC, voltage sensing and current sensing, and advanced haptic algorithms running on an on-chip 24-bit 100 MHz dual-MAC DSP.
- Very competitive PCB footprint ($< 16 \text{ mm}^2$).
- 100 % compatible with Android haptic/vibration APIs
- Automatic transducer diagnosis and calibration at production line without human engagement.
- Run-time transducer model (f_0) tracking after production.
- Run-time transducer distortion and temperature control.
- On-chip autonomous boot-up vibration playback.
- On-chip resonant drive signal (buzz/tone) generation with boosting and braking.
- On-chip click effect (for virtual buttons, etc.) via wave table playback.
- Real-time playback for haptic effect streams (I²S/TDM).
- Audio display support (voice call without receiver speaker. Using LRA in place of the speaker) for intelligible speech playback.
- Embedded sequencer (Goodix Technology driver support), to enable complex haptic sequences.
- Audio-to-Haptics total solution for gaming experience enhancement with major SOC platforms.
- Supports size-limited low impedance transducers down to 8Ω .
- Battery protection with minimal risk of black-out.
- Audio grade drive signal generation without hearable noise.
- Automatic power state management.
- High output power: 5.6 W (AVG) to 8Ω at 4.0 V supply voltage (THD = 1 %; $V_{BST} = 10 \text{ V}$).
- Supports 8Ω to 32Ω load configurations.
- High efficiency, low power dissipation, and low noise haptic driver (dynamic range $> 110 \text{ dB}$).
- Adaptive DC-to-DC converter which, when switching between fixed boost and adaptive boost mode, increases the supply voltage smoothly, preventing large battery supply spikes and limiting quiescent power consumption.
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V).
- Very low noise output (typ: $14 \mu\text{V}$ with null DATA input at $f_s = 48 \text{ kHz}$).
- I²C-bus control interface (400 kHz).
- Haptic current and voltage monitoring.
- 48 kHz dedicated sample frequency
- Configurable full duplex 4-wire TDM input interface.
- Programmable interrupt control via a dedicated interrupt pin.
- Thermal foldback and overtemperature protection.
- 15 kV system-level ESD protection without external components on amplifier output.

3 Applications

- Mobile phones and tablets
- Portable gaming devices
- Portable navigation devices (PND)

4 Quick reference data

Table 4-1: Quick reference data

All parameters are guaranteed for $V_{BAT} = 4.0\text{ V}$; $V_{DDD} = V_{DDE} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10\text{ V}$, adaptive boost mode;
 $L_{BST} = 1\ \mu\text{H}^{[1]}$; $R_L = 8\ \Omega^{[1]}$; $L_L = 44\ \mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--------------------------------|--|------|------|------|---------------|
| V_{BAT} | battery supply voltage | on pin V_{BAT} ; In application, V_{BAT} must not be lower than V_{DDD} levels | 2.7 | - | 5.5 | V |
| V_{DDD} | digital supply voltage | on pin V_{DDD} | 1.65 | 1.8 | 1.95 | V |
| V_{DDE} | digital supply voltage | on pin V_{DDE} | 1.65 | 1.8 | 1.95 | V |
| V_{DDP} | power supply voltage | on pin V_{DDP} | 2.7 | - | 10.2 | V |
| R_L | load impedance | | 8 | 16 | 32 | Ω |
| $f_{rsn(tr)}$ | transducer resonance frequency | | 120 | 160 | 1000 | Hz |
| I_{BAT} | battery supply current | active state; on pin V_{BAT} ; operating mode with load $R_L = 8\ \Omega$; DC-to-DC in adaptive boost mode; $P_o = 600\text{ mW}$; $V_{BAT} = 4.0\text{ V}$; $V_{DDP} = 10\text{ V}$; 100 Hz sine wave; running on MCLK (19.2 MHz) | - | 165 | - | mA |
| | | idle state; on pin V_{BAT} ; operating mode with load $R_L = 8\ \Omega$ and no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; $V_{BAT} = 4.0\text{ V}$; low power mode enabled; Running on MCLK (19.2 MHz) | - | 2.7 | - | mA |
| | | power-down state; on pin V_{BAT} ; DC-to-DC in power-down mode; $T_j = 25\text{ }^\circ\text{C}$; running on MCLK (19.2 MHz). | - | 1 | - | μA |
| I_{DDD} | digital supply current | active state (DSP Running); on pin V_{DDD} ; operating mode with load $R_L = 8\ \Omega$; DC-to-DC in adaptive boost mode; $P_o = 600\text{ mW}$; $V_{BAT} = 4.0\text{ V}$; $V_{DDP} = 10\text{ V}$; 100 Hz sine wave; running on MCLK (19.2 MHz) | - | 11.2 | - | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--------------|--------------------------------------|--|------|-------|------|---------------|---------------|
| | | idle state (DSP Disabled); on pin VDDD; operating mode with load $R_L = 8 \Omega$ and no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; $V_{BAT} = 4.0 \text{ V}$; low power mode enabled; running on MCLK (19.2 MHz) | - | 3.9 | - | mA | |
| | | power-down state; on pin VDDD; DC-to-DC in power-down mode; $T_j = 25 \text{ }^\circ\text{C}$; running on MCLK (19.2 MHz). | - | 124 | - | μA | |
| $P_{O(AVG)}$ | average output power | THD+N = 1 %; ($R_L = 8 \Omega$; $L_L = 44\mu\text{H}$); $V_{BST} = 10 \text{ V}$; $V_{BAT} = 4.0 \text{ V}$; $V_{DDD} = 1.8 \text{ V}$ | 5.3 | 5.6 | - | W | |
| | | THD+N = 1 %; ($R_L = 32 \Omega$; $L_L = 30\mu\text{H}$); $V_{BST} = 10 \text{ V}$; $V_{BAT} = 4.0 \text{ V}$; $V_{DDD} = 1.8 \text{ V}$ | 1.1 | 1.5 | - | W | |
| THD+N | total harmonic distortion-plus-noise | $P_o = 2.0 \text{ W}$; $R_L = 8 \Omega$; $L_L = 44 \mu\text{H}$ | - | 0.015 | 0.09 | % | |
| ΔG | gain variation over frequency | $BW = 20 \text{ Hz to } 15 \text{ kHz}$; $V_{BAT} = 3.4 \text{ V to } 5 \text{ V}$; $P_o = 2.0 \text{ W}$ | -0.1 | - | +0.7 | dB | |
| V_{POP} | pop noise | at mode transition and gain change; with $C_L < 200 \text{ pF}$ | [2] | - | 2 | mV | |
| $V_{n(o)}$ | output noise voltage | a-weighted; no input signal; low noise mode | [3] | - | 14 | 18 | μV |
| DR | dynamic range | a-weighted; $V_{BAT} = 3.4 \text{ V to } 5 \text{ V}$; S/N = maximum signal (at THD = 1 %) – output noise voltage ($V_{n(o)}$); no signal applied | 110 | 114 | - | dB | |
| S/N | signal-to-noise ratio | a-weighted; $V_{BAT} = 3.4 \text{ V to } 5 \text{ V}$; S/N = maximum signal (at THD = 1 %) – output noise voltage ($V_{n(o)}$); signal applied | 100 | - | - | dB | |
| η_{po} | output power efficiency | on pin V_{BAT} ; input: 100 Hz sine wave; DC-to-DC in adaptive boost mode; $V_{BAT} = 4.0 \text{ V}$; $V_{DDP} = 10 \text{ V}$; $P_o = 4 \text{ W}$ | - | 82 | - | % | |

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] When C_L exceeds 200 pF, low power mode must be disabled.

[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

5 Ordering information

Table 5-1: Ordering information

| Type number | Package | | |
|---------------|---------|---|-----------|
| | Name | Description | Version |
| TFA9914UK/N1 | WLCSP48 | wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm × 3.55 mm × 0.50 mm body; no backside coating | SOT1887-2 |
| TFA9914BUK/N1 | WLCSP48 | wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm × 3.55 mm × 0.50 mm body; backside coating | SOT1887-3 |

7 Pinning information

7.1 Pinning

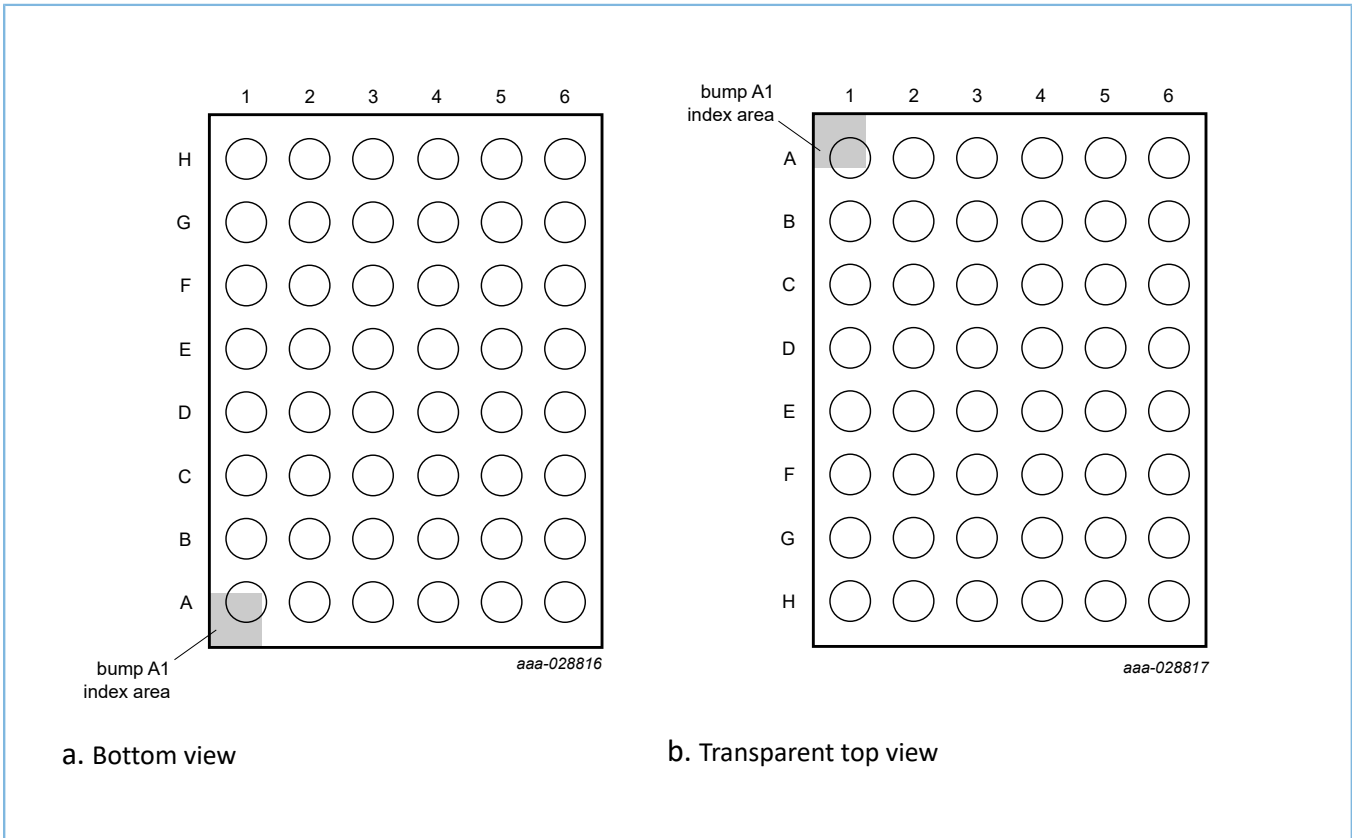


Figure 7-1: Bump configuration

| | | | | | | |
|---|-------|-------|------|-------|-------|-------|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| A | MCLK | VDDE | VDDD | GNDD | GNDD | GNDD |
| B | GNDD | FS | VDDD | SCL | GNDD | GNDD |
| C | BCK | FS | VDDD | SCL | SDA | TRSTN |
| D | DATAO | DATAI | ADS2 | ADS1 | INT | VBAT |
| E | RST | GNDD | VSN | TEST2 | TEST1 | VSP |
| F | GNDB | GNDB | GNDB | GNDD | GNDD | GNDD |
| G | INB | INB | INB | OUTP | GNDD | OUTN |
| H | VBST | VBST | VBST | VDDP | VDDP | VDDP |

aaa-028818

Transparent top view

Figure 7-2: Bump mapping

Table 7-1: Pinning

| Symbol | Pin | Type | Description |
|--------|-----|------|--|
| MCLK | A1 | I | master clock input |
| VDDE | A2 | P | pad digital supply voltage (to be connected to VDDD) |
| VDDD | A3 | P | digital supply voltage |
| GNDD | A4 | P | digital ground |
| GNDD | A5 | P | digital ground |
| GNDD | A6 | P | digital ground |
| GNDD | B1 | P | digital ground |
| FS | B2 | I | digital data frame sync for TDM interface |
| VDDD | B3 | P | digital supply voltage |
| SCL | B4 | I | digital I ² C-bus clock input |
| GNDD | B5 | P | digital ground |
| GNDD | B6 | P | digital ground |
| BCK | C1 | I | digital data bit clock input for TDM interface |
| FS | C2 | I | digital data frame sync for TDM interface |

| Symbol | Pin | Type | Description |
|--------|-----|------|---|
| VDDD | C3 | P | digital supply voltage |
| SCL | C4 | I | digital I ² C-bus clock input |
| SDA | C5 | I/O | digital I ² C-bus data input/output |
| TRSTN | C6 | I | test signal input TRSTN, connect to PCB ground |
| DATAO | D1 | O | digital data data output for TDM interface |
| DATAI | D2 | I | digital data data input for TDM interface |
| ADS2 | D3 | I | digital address select input 2 |
| ADS1 | D4 | I | digital address select input 1 |
| INT | D5 | O | digital interrupt output |
| VBAT | D6 | P | battery supply voltage |
| RST | E1 | I | digital reset input |
| GNDD | E2 | P | digital ground |
| VSN | E3 | I/O | voltage sensing inverting |
| TEST2 | E4 | I/O | test signal IO 2; for test purposes only, connect to PCB ground |
| TEST1 | E5 | I/O | test signal IO 1; for test purposes only, connect to PCB ground |
| VSP | E6 | I/O | voltage sensing non-inverting |
| GNDB | F1 | P | booster ground |
| GNDB | F2 | P | booster ground |
| GNDB | F3 | P | booster ground |
| GNDD | F4 | P | digital ground |
| GNDP | F5 | P | power ground |
| GNDD | F6 | P | digital ground |
| INB | G1 | P | DC-to-DC boost converter input |
| INB | G2 | P | DC-to-DC boost converter input |
| INB | G3 | P | DC-to-DC boost converter input |
| OUTP | G4 | P | non-inverting output |
| GNDP | G5 | P | power ground |
| OUTN | G6 | P | inverting output |

| Symbol | Pin | Type | Description |
|--------|-----|------|-------------------------------|
| VBST | H1 | O | boosted supply voltage output |
| VBST | H2 | O | boosted supply voltage output |
| VBST | H3 | O | boosted supply voltage output |
| VDDP | H4 | P | power supply voltage |
| VDDP | H5 | P | power supply voltage |
| VDDP | H6 | P | power supply voltage |

8 Functional description

The TFA9914 is a highly efficient bridge-tied load (BTL) class-D amplifier for Haptic, depicted in block diagram of [Figure 6-1](#).

TFA9914 contains a TDM input/output interface for communicating with the host. The interface is compliant with standard TDM interfaces and supports a wide range of configurations. It can be configured to output current sense and voltage sense information, which can be further used by the host.

The Haptic pattern generation is automatically handled by the embedded Coolflux digital signal processor (DSP) together with dedicated libraries running on host. It supports the following haptic features:

- Wave table playback: prestored pattern playback from embedded wave pattern table
- Tone generator: resonant tone playback with resonant frequency (f_0) tracking at ± 2 Hz accuracy
- Automatic boost/brake effect for fast ramp-up/ramp-down and ringing compensation
- TDM real-time streaming support (for external pattern playback)
- Concurrent playback of tone generator, wavetable, and streaming inputs
- Dedicated sequencer for complex haptic feedback
- Preprocessing libraries (available from Goodix for host execution) supporting Audio-to-Haptics (gaming and multimedia experience enhancement) and Audio-Display (voice call handset mode with LRA in place for a regular RCV speaker).

At low battery voltage levels, the output level is automatically clipped to limit battery current (when battery safeguard is enabled).

The digital data stream is converted into two pulse width modulated (PWM) signals which are then injected into the class-D amplifier. The 3-level PWM scheme supports filterless haptic drive.

When the data stream crosses a programmable voltage threshold, an adaptive DC-to-DC converter boosts the battery supply voltage. When boosting, the DC-to-DC provides a boosted supply in line with the data signal. In this mode, 2 configurations are available (Two-levels mode or Tracking mode (default)).

9 I²C-bus interface and register settings

The TFA9914 supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control the TFA9914 and to transmit and receive data. The TFA9914 can only operate in I²C slave mode, as a slave receiver or as a slave transmitter.

9.1 TFA9914 addressing

The TFA9914 is accessed via an 8-bit code (see [Table 9-1](#)). Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address, as detailed in [Table 9-1](#). The generic address is independent of pins ADS1 and ADS2.

Table 9-1: Address selection via pins ADS1 and ADS2

| ADS2 pin voltage (V) | ADS1 pin voltage (V) | Address | Function |
|----------------------|----------------------|----------------------------|----------------|
| 0 | 0 | 01101000 | for write mode |
| | | 01101001 | for read mode |
| 0 | V _{DDD} | 01101010 | for write mode |
| | | 01101011 | for read mode |
| V _{DDD} | 0 | 01101100 | for write mode |
| | | 01101101 | for read mode |
| V _{DDD} | V _{DDD} | 01101110 | for write mode |
| | | 01101111 | for read mode |
| do not care | do not care | 00011100 (generic address) | for write mode |
| do not care | do not care | 00011101 (generic address) | for read mode |

9.2 I²C-bus write cycle

The sequence of events that must be followed when writing data to the I²C-bus registers of the TFA9914 is detailed in [Table 9-2](#). One byte is transmitted at a time. Each register stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9914, followed by the R/W bit set to 0.
3. The TFA9914 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9914 register address to which the first data byte is written.

5. The TFA9914 asserts an acknowledge.
6. The microcontroller transmits the first byte (the most significant byte).
7. The TFA9914 asserts an acknowledge.
8. The microcontroller transmits the second byte (the least significant byte).
9. The TFA9914 asserts an acknowledge.
10. The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address has been auto-incremented by the TFA9914.

Table 9-2: I²C-bus write cycle

| Start | TFA9914 address | R/W | | TFA9914 first register address | | MSB | | LSB | | More data... | Stop |
|-------|------------------------------------|-----|---|--------------------------------|---|-----|---|-----|---|--------------|------|
| S | 01101A ₂ A ₁ | 0 | A | ADDR | A | MS1 | A | LS1 | A | <....> | P |

9.3 I²C-bus read cycle

The sequence of events that must be followed when reading data from the I²C-bus registers of the TFA9914 is detailed in [Table 9-3](#). One byte is transmitted at a time. Each of the registers stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9914, followed by the R/W bit set to 0.
3. The TFA9914 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9914 register address from which the first data byte is read.
5. The TFA9914 asserts an acknowledge.
6. The microcontroller asserts a repeated start (Sr).
7. The microcontroller retransmits the device address followed by the R/W bit set to 1.
8. The TFA9914 asserts an acknowledge.
9. The TFA9914 transmits the first byte (the MSB).
10. The microcontroller asserts an acknowledge.
11. The TFA9914 transmits the second byte (the LSB).
12. The microcontroller asserts either an acknowledge or a negative acknowledge (NA).
 - If the microcontroller asserts an acknowledge, the target register address is auto-increased by the TFA9914 and steps 9 to 12 are repeated.

- If the microcontroller asserts a negative acknowledge, the TFA9914 frees the I²C-bus and the microcontroller generates a stop condition (P).

Table 9-3: I²C-bus read cycle

| Start | TFA9914 address | R/W | | First register address | | | TFA9914 address | R/W | | MSB | | LSB | | More data... | | Stop |
|-------|------------------------------------|-----|---|------------------------|---|----|------------------------------------|-----|---|-----|---|-----|---|--------------|----|------|
| S | 01101A ₂ A ₁ | 0 | A | ADDR | A | Sr | 01101A ₂ A ₁ | 1 | A | MS1 | A | LS1 | A | <....> | NA | P |

10 Limiting values

Table 10-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------------------|--|---------------------|-----|------|------|
| V _{BAT} | battery supply voltage | on pin V _{BAT} | -0.3 | - | +6 | V |
| V _{BST} | booster output voltage | on pin V _{BST} | -0.3 | - | +12 | V |
| V _{INB} | booster input voltage | on pin INB | ^[1] -0.3 | - | +12 | V |
| V _{DDP} | power supply voltage | on pin V _{DDP} | -0.3 | - | +12 | V |
| V _{OUTX} | voltage on amplifier connections | on pin OUTN, OUTP | ^[1] -0.3 | - | +12 | V |
| V _{DDD} | digital supply voltage | on pin V _{DDD} | -0.3 | - | +2.5 | V |
| V _{DDE} | digital supply voltage | on pin V _{DDE} | -0.3 | - | +2.5 | V |
| V _{LTESTX} | low-voltage test pins | on pin TEST1/TEST2 | -0.3 | - | +6 | V |
| V _{HVSX} | high-voltage pins | on pin VSP, VSN | ^[1] -0.3 | - | +12 | V |
| T _j | junction temperature | | - | - | +125 | °C |
| T _{stg} | storage temperature | | -55 | - | +150 | °C |
| T _{amb} | ambient temperature | | -40 | - | +85 | °C |
| V _{ESD} | electrostatic discharge voltage | according to human body model (HBM) | -2 | - | +2 | kV |
| | | according to charge device model (CDM) | -500 | - | +500 | V |

[1] Using Goodix demo board, with a 1 mm wire/PCB track lengths, AC pulse from -6 V to +15 V can be observed on INB, OUTP, OUTN, VSP, VSN without damaging the device as these spikes do not end up inside the actual device.

11 Thermal characteristics

Table 11-1: Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|---------------------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | 4-layer application board | 37 | K/W |

12 Characteristics

12.1 DC characteristics

Table 12-1: DC characteristics

All parameters are guaranteed for $V_{BAT} = 4.0\text{ V}$; $V_{DDD} = V_{DDE} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10\text{ V}$, adaptive boost mode; $L_{BST} = 1\text{ }\mu\text{H}^{[1]}$; $R_L = 8\text{ }\Omega^{[1]}$; $L_L = 44\text{ }\mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|------------------------|--|-----|-----|------|---------------|
| V_{BAT} | battery supply voltage | on pin V_{BAT} ; in application, V_{BAT} must not be lower than V_{DDD} | 2.7 | - | 5.5 | V |
| I_{BAT} | battery supply current | active state; on pin V_{BAT} ; operating mode with load $R_L = 8\text{ }\Omega$; DC-to-DC in adaptive boost mode; $P_o = 600\text{ mW}$; $V_{BAT} = 4.0\text{ V}$; $V_{DDP} = 10\text{ V}$; 100 Hz sine wave; running on MCLK (19.2 MHz) | - | 165 | - | mA |
| | | idle state; on pin V_{BAT} ; operating mode with load $R_L = 8\text{ }\Omega$; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; $V_{BAT} = 4.0\text{ V}$; low-power mode enabled; running on MCLK (19.2 MHz) | - | 2.7 | - | mA |
| | | Idle state on pin V_{BAT} ; operating mode with load $R_L = 8\text{ }\Omega$; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; $V_{BAT} = 4.0\text{ V}$; low-power mode disabled; running on MCLK (19.2 MHz) | - | 5.7 | - | mA |
| | | power-down state; on pin V_{BAT} ; DC-to-DC in power-down mode. $T_j = 25\text{ }^\circ\text{C}$; running on MCLK (19.2 MHz). | - | 1 | - | μA |
| V_{DDP} | power supply voltage | on pin V_{DDP} | 2.7 | - | 10.2 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--------------------------|---|---------------------|------|---------------------|------|
| V _{DDD} | digital supply voltage | on pin V _{DDD} | 1.65 | 1.8 | 1.95 | V |
| V _{DDE} | digital supply voltage | on pin V _{DDE} | 1.65 | 1.8 | 1.95 | V |
| I _{DDD} | digital supply current | active state (DSP running); on pin V _{DDD} ; operating mode with load R _L = 8 Ω; DC-to-DC in adaptive boost mode, P _o = 600 mW; V _{BAT} = 4.0 V; V _{DDP} = 10 V; 100 Hz sine wave; running on MCLK (19.2 MHz) | - | 11.2 | - | mA |
| | | idle state (DSP disabled); on pin V _{DDD} ; operating mode with load R _L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V _{BAT} = 4.0 V; low-power mode enabled; running on MCLK (19.2 MHz) | - | 3.9 | - | mA |
| | | idle state (DSP disabled); on pin V _{DDD} ; operating mode with load R _L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V _{BAT} = 4.0 V; low-power mode disabled; running on MCLK (19.2 MHz) | - | 5.2 | - | mA |
| | | power-down state; on pin V _{DDD} ; DC-to-DC in power-down mode; T _j = 25 °C; running on MCLK (19.2 MHz). | - | 124 | - | μA |
| Pins FS, BCK, DATAI, ADS1, ADS2, SCL, SDA, RST, TRST, MCLK (input) | | | | | | |
| V _{IH} | HIGH-level input voltage | | 0.7V _{DDD} | - | V _{DDD} | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{DDD} | V |
| C _{in} | input capacitance | | ^[2] - | - | 3 | pF |
| I _{LI} | input leakage current | 1.8 V on input pin | - | - | 0.1 | μA |
| | | 1.8 V on input pin RST; (90 kΩ pull-down) | - | 90 | 120 | μA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--|-----------------------|-----|------|--------------|
| | | 1.8 V on input pin TRST; (20 k Ω pull-down) | - | 20 | 30 | μ A |
| Pins DATA0, INT push-pull output stages (output) | | | | | | |
| V _{OH} | HIGH-level output voltage | I _{OH} = 4 mA | V _{DD} - 0.4 | - | - | V |
| V _{OL} | LOW-level output voltage | I _{OL} = 4 mA | - | - | 400 | mV |
| Pins SDA, open-drain outputs, external 10 kΩ resistor to V_{DD} | | | | | | |
| V _{OH} | HIGH-level output voltage | I _{OH} = 4 mA | V _{DD} - 0.4 | - | - | V |
| V _{OL} | LOW-level output voltage | I _{OL} = 4 mA | - | - | 400 | mV |
| Pins OUTP, OUTN | | | | | | |
| R _{DSon} | total drain-source on-state resistance | (PMOS+NMOS transistors) | - | 430 | 520 | m Ω |
| Protection | | | | | | |
| T _{act(th_prot)} | thermal protection activation temperature | | 130 | - | - | $^{\circ}$ C |
| V _{uvp(VBAT)} | undervoltage protection on pin VBAT | | 2.3 | - | 2.7 | V |
| I _{O(ocp)} | overcurrent protection output current | | 2.5 | - | - | A |
| DC-to-DC converter | | | | | | |
| V _{BST} | voltage on pin V _{BST} | DCVOS = "111111"; fixed boost mode and switching amplifier | 9.8 | 10 | 10.2 | V |

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

12.2 AC characteristics

Table 12-2: AC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 μ H^[1]; R_L = 8 Ω ^[1]; L_L = 44 μ H^[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 $^{\circ}$ C; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------|-------------|-----|-----|-----|------|
| Amplifier output power | | | | | | |
| P _{o(AVG)} | average output power | THD+N = 1 % | | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|---|--|------------|------|-------|------|---------------|
| | | $R_L = 8 \Omega$; $L_L = 44 \mu\text{H}$; $V_{\text{BAT}} = 4.0 \text{ V}$ | 5.30 | 5.60 | - | W | |
| | | $R_L = 32 \Omega$; $L_L = 30 \mu\text{H}$; $V_{\text{BAT}} = 4.0 \text{ V}$ | 1.10 | 1.50 | - | W | |
| Amplifier output pins (OUTP and OUTN) | | | | | | | |
| $ V_{\text{O(offset)}} $ | output offset voltage after trimming | absolute value, after trimming; $V_{\text{DDP}} = 3.4 \text{ V}$ to 10 V ; $V_{\text{BAT}} = 3.4 \text{ V}$ to 5 V | - | - | 1.0 | mV | |
| Amplifier performances | | | | | | | |
| η_{po} | output power efficiency | on pin V_{BAT} ; input: 100 Hz sine wave; DC-to-DC in adaptive boost mode, $V_{\text{BAT}} = 4.0 \text{ V}$; $P_{\text{O}} = 600 \text{ mW}$ | [2] | - | 91 | - | % |
| | | on pin V_{BAT} ; input: 100 Hz sine wave; DC-to-DC in adaptive boost mode; $V_{\text{BAT}} = 4.0 \text{ V}$; $P_{\text{O}} = 4 \text{ W}$ | [2] | - | 82 | - | % |
| THD+N | total harmonic distortion-plus-noise | $P_{\text{O}} = 2.0 \text{ W}$; $R_L = 8 \Omega$; $L_L = 44 \mu\text{H}$ | [3] | - | 0.015 | 0.09 | % |
| | | $P_{\text{O}} = 0.1 \text{ W}$; $R_L = 32 \Omega$; $L_L = 44 \mu\text{H}$ | [3] | - | 0.04 | 0.09 | % |
| $V_{\text{n(o)}}$ | output noise voltage | a-weighted; no input signal; low noise mode; | [2] [4] | - | 14 | 18 | μV |
| DR | dynamic range | a-weighted; $V_{\text{BAT}} = 3.4 \text{ V}$ to 5 V ; $S/N = \text{maximum signal (at THD} = 1\%) - \text{output noise voltage (} V_{\text{n(o)}}\text{)}$; no signal applied | [2] | 110 | 114 | - | dB |
| S/N | signal-to-noise ratio | a-weighted; $V_{\text{BAT}} = 3.4 \text{ V}$ to 5 V ; $S/N = \text{maximum signal (at THD} = 1\%) - \text{output noise voltage (} V_{\text{n(o)}}\text{)}$; signal applied | [2] | 100 | - | - | dB |
| PSRR | power supply rejection ratio (from V_{BAT}) | booster in follower mode ($V_{\text{DDP}} = V_{\text{BAT}}$); $f_{\text{ripple}} = 217 \text{ Hz}$ square wave; $V_{\text{ripple}} = 50 \text{ mV}_{\text{pp}}$; $V_{\text{BAT}} = 4.0 \text{ V}$ | | 70 | 80 | - | dB |
| | | booster in follower mode ($V_{\text{DDP}} = V_{\text{BAT}}$); $f_{\text{ripple}} = 20 \text{ Hz}$ to 1 kHz sine wave; $V_{\text{ripple}} = 200 \text{ mV}_{\text{RMS}}$; $V_{\text{BAT}} = 3.4 \text{ V}$ to 5.0 V | | 70 | 80 | - | dB |
| | | booster in follower mode ($V_{\text{DDP}} = V_{\text{BAT}}$); $f_{\text{ripple}} = 1 \text{ kHz}$ to 20 kHz sine wave; $V_{\text{ripple}} = 200 \text{ mV}_{\text{RMS}}$; $V_{\text{BAT}} = 3.4 \text{ V}$ to 5.0 V | | 55 | 64 | - | dB |
| ΔG | gain variation over frequency | $\text{BW} = 20 \text{ Hz}$ to 15 kHz ; $V_{\text{BAT}} = 3.4 \text{ V}$ to 5 V ; $P_{\text{O}} = 2.0 \text{ W}$ | | -0.1 | - | +0.7 | dB |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|-------|------|------|------|
| V _{POP} | pop noise | at mode transition and gain change; with C _L < 200 pF | [5] - | - | 2 | mV |
| R _L | load resistance | | 8 | 16 | 32 | Ω |
| f _{r_{sn}(tr)} | transducer resonance frequency | | 120 | 160 | 1000 | Hz |
| C _L | load capacitance | | [5] - | 200 | 1000 | pF |
| L _L | load inductance | | 30 | - | - | μH |
| f _{sw} | switching frequency | directly coupled to the TDM input frequency | - | 384 | - | kHz |
| G _(TDM-VO) | TDM to V _O gain | INPLEV = 0 dB | 6 | - | 21 | dBV |
| | | INPLEV = -6 dB | 0 | - | 15 | dBV |
| Amplifier power-up, power-down, and propagation delays | | | | | | |
| t _{d(on)PLL} | PLL turn-on delay time | PLL locked on BCK | - | 1.3 | - | ms |
| | | PLL locked on FS | - | 0.3 | - | ms |
| | | PLL locked on MCLK | - | 1.3 | - | ms |
| t _{d(on)amp} | amplifier turn-on delay time | | [6] - | 55 | - | μs |
| t _{d(pd)} | turn-off delay time | | - | 115 | - | μs |
| t _{d(alarm)} | alarm delay time | | - | 300 | - | ms |
| t _{PD} | propagation delay | | [4] - | 650 | 700 | μs |
| Booster inductance | | | | | | |
| L | inductance | | 0.33 | 1.0 | 2.2 | μH |
| f _{s(bst)} | boost switching frequency | fixed boost; V _{DDP} = 10 V; I _{load} = 1 A; f _s = 48 kHz | - | 2.05 | | MHz |
| Current-sensing performance | | | | | | |
| ΔV _{sense} /I _{sense} | V _{sense} /I _{sense} ratio mismatch | pilot tone = 100 mVpk | [7] - | 2 | - | % |
| THD+N | total harmonic distortion-plus-noise | on current sensing; V _{in} = -12 dBFS | - | - | 0.75 | % |
| S/N | signal-to-noise ratio | on current sensing; I _o = 1 A (peak); a-weighted | 62 | 65 | - | dB |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|------------------------|-----------------|----------|-------|-----|---------|
| Brownout detection (BOD) | | | | | | |
| $V_{th(BOD)}$ | BOD threshold voltage | BODTHLVL = "10" | [8] 1.55 | 1.575 | 1.6 | V |
| $V_{hys(BOD)}$ | BOD hysteresis voltage | BODHYS = 1 | - | 20 | - | mV |
| $t_{t(BOD)}$ | BOD delay time | BODFILT = "10" | - | 10 | - | μ s |
| Clocks | | | | | | |
| $t_{jit(p-p)}$ | input clock jitter | MCLK | - | 0.5 | 1.0 | ns |
| | | BCK (3.072 MHz) | - | 1.0 | 2.0 | ns |
| | | FS | [9] | - | - | 20 |
| $\delta_{i(clk)}$ | clock input duty cycle | MCLK | 40 | - | 60 | % |

- [1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
- [2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
- [3] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance.
- [4] Only supports $f_s = 48$ kHz.
- [5] When C_L exceeds 200 pF, low-power mode must be disabled.
- [6] At power-up, data is output on OUTP/OUTN after $t_{d(on)amp} + t_{d(on)PLL}$.
- [7] Intended for temperature protection. In combination with Goodix Technology temperature protection, a temperature accuracy of ± 10 °C can be realized.
- [8] Recommended setting.
- [9] When the PLL is locked on FS, the system is less sensitive to jitter.

12.3 TDM timing characteristics

Table 12-3: TDM bus interface characteristics

All parameters are guaranteed for $V_{BAT} = 4.0$ V; $V_{DD} = V_{DDE} = 1.8$ V; $V_{DDP} = V_{BST} = 10$ V, adaptive boost mode; $L_{BST} = 1$ μ H^[1]; $R_L = 8$ Ω ^[1]; $L_L = 44$ μ H^[1]; $f_i = 1$ kHz; $f_s = 48$ kHz; $T_{amb} = 25$ °C; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--------------------|-----------------------|-------------|-----|----------|------|
| f_s | sampling frequency | on pin FS | [2] - | 48 | - | kHz |
| f_{clk} | clock frequency | on pin BCK | [2] $32f_s$ | - | $384f_s$ | kHz |
| t_{su} | set-up time | FS edge to BCK HIGH | [3] 10 | - | - | ns |
| | | DATA edge to BCK HIGH | 10 | - | - | ns |
| t_h | hold time | BCK HIGH to FS edge | [3] 10 | - | - | ns |
| | | BCK HIGH to DATA edge | 10 | - | - | ns |

- [1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
- [2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. The BCK and FS signals must be present for the clock to operate correctly.
- [3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation

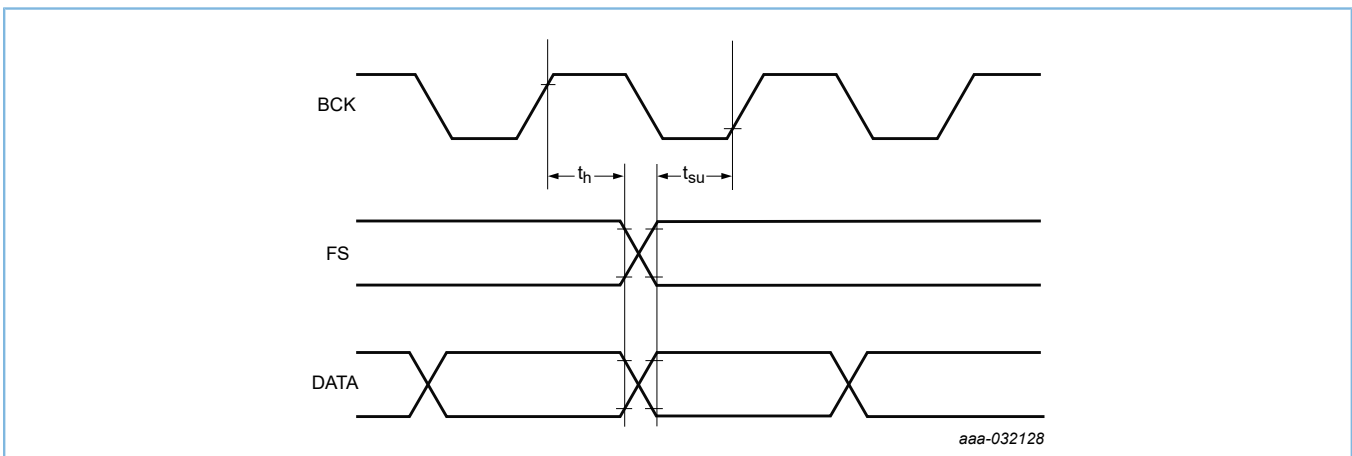


Figure 12-1: TDM timing

12.4 I²C timing characteristics

Table 12-4: I²C-bus interface characteristics

All parameters are guaranteed for $V_{BAT} = 4.0\text{ V}$; $V_{DDD} = V_{DDE} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10\text{ V}$, adaptive boost mode; $L_{BST} = 1\text{ }\mu\text{H}^{[1]}$; $R_L = 8\text{ }\Omega^{[1]}$; $L_L = 44\text{ }\mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|--|---------------------|------------------------------|-----|-----|---------------|
| f_{SCL} | SCL clock frequency | | - | - | 400 | kHz |
| t_{LOW} | LOW period of the SCL clock | | 1.3 | - | - | μs |
| t_{HIGH} | HIGH period of the SCL clock | | 0.6 | - | - | μs |
| t_r | rise time | SDA and SCL signals | ^[2] $20 + 0.1C_b$ | - | - | ns |
| t_f | fall time | SDA and SCL signals | ^[2] $20 + 0.1C_b$ | - | - | ns |
| $t_{HD,STA}$ | hold time (repeated) START condition | | ^[3] 0.6 | - | - | μs |
| $t_{SU,STA}$ | set-up time for a repeated START condition | | 0.6 | - | - | μs |
| $t_{SU,STO}$ | set-up time for STOP condition | | 0.6 | - | - | μs |
| t_{BUF} | bus free time between a STOP and START condition | | 1.3 | - | - | μs |
| $t_{SU,DAT}$ | data set-up time | | 100 | - | - | ns |
| $t_{HD,DAT}$ | data hold time | | 0 | - | - | μs |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---|------------|-------|-----|-----|------|
| t_{SP} | pulse width of spikes that must be suppressed by the input filter | | [4] 0 | - | 50 | ns |
| C_b | capacitive load for each bus line | | - | - | 400 | pF |

- [1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
- [2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
- [3] After this period, the first clock pulse is generated.
- [4] To be suppressed by the input filter.

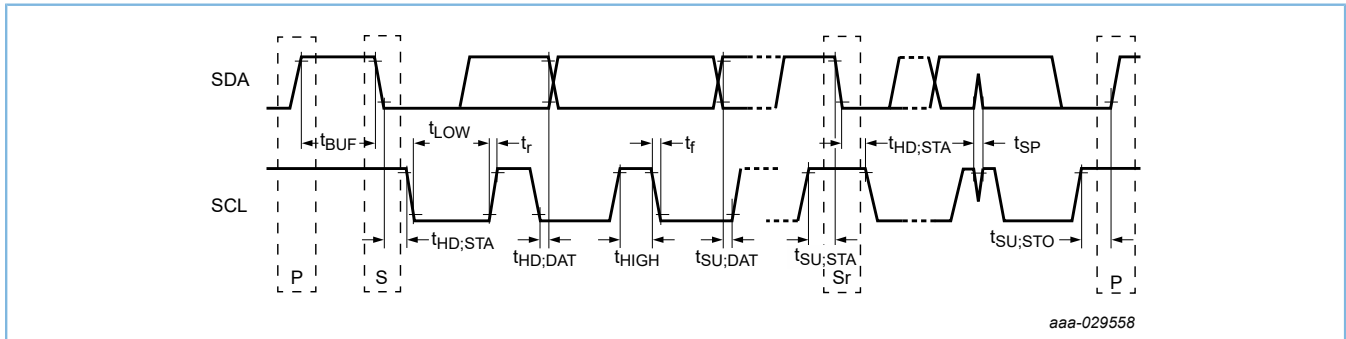


Figure 12-2: I2C timing

13 Application information


13.1 External components

The DC-to-DC converter requires a battery supply voltage capacitor (C_{VBAT}), an output capacitor (C_{VDDP}), and an inductor (L_{BST}) to work properly. The nominal values of these components are 22 μF , 33 μF , and 1 μH , respectively. If a larger coil is used, the capacitance must also be increased. A 1 μF decoupling capacitor (C_{VDD}) must be connected close to the V_{DD} pin. The V_{DE} pin must be connected externally to the V_{DD} pin. One 4.7 k Ω resistor, R_{VS} , must be connected between each voltage sensing input and its corresponding amplifier output ($VSP/OUTP$ and $VSN/OUTN$).

13.1.1 DC-to-DC converter output capacitor

A ceramic capacitor is required at the output of the DC-to-DC converter (C_{VDDP}).

Capacitors constructed using X5R (-55 °C to +85 °C) or X7R (-55 °C to +125 °C) dielectric materials are preferred because they are compact, feature low ESR and are sufficiently stable over a wide temperature range. The capacitance value decreases over the DC biasing voltage range (50 % to 85 % decrease). Consequently, the selected capacitor must have a nominal value three to four times higher than the required minimum effective capacitance.

 **Note:** The DC-to-DC converter capacitor connected to pin VBST (C_{VDDP}) is critical for stability. The recommended effective value (the capacitance value at the maximum boost voltage) of C_{VDDP} depends on the coil inductance, and is given in [Table 13-1](#). The position of the capacitor and the layout of the board are also critical. Connect C_{VDDP} as close as possible to the BST and GNDB pins without vias in the PCB tracks.

In many applications, it is desirable to limit the height of components as much as possible. Limiting the height of the components can be achieved for C_{VDDP} by placing two smaller capacitors in parallel. The rated voltage must be 10 V or higher.

Table 13-1: DC-to-DC minimum output capacitor

| Effective coil value (at maximum current) | | Minimum effective capacitance (at the boost voltage) |
|---|-----|--|
| 0.47 μH | | 3.4 μF |
| 1 μH | [1] | 4 μF |
| 1.5 μH | | 12 μF |
| 2.2 μH | | 20 μF |

[1] Recommended value. Higher values are not preferred because of the cost and space required for the coil (L_{BST}) and the capacitor (C_{VDDP}).

The values in the [Table 13-2](#) and [Table 13-3](#) are guaranteed for capacitors rated X5R or higher.

Table 13-2: DC-to-DC recommended output capacitor

| Specification | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---|-----|-----|-----|---------------|
| nominal capacitance; 20 % tolerance | 6 Ω or 8 Ω load; 1 μH inductor (L_{BST}) | - | 33 | - | μF |
| minimum effective capacitance | | 4 | - | - | μF |

| Specification | Conditions | Min | Typ | Max | Unit |
|---------------|------------|-----|-----|-----|------|
| rated voltage | | 10 | - | - | V |

13.1.2 Battery capacitor

C_{VBAT} must be at least half the value of C_{VDDP} .

Table 13-3: Battery recommended capacitor

| Specification | Min | Typ | Max | Unit |
|-------------------------------------|-----|-----|-----|---------------|
| nominal capacitance; 20 % tolerance | - | 22 | - | μF |
| rated voltage | 10 | - | - | V |

13.1.3 DC-to-DC converter inductor

An inductor is required at the output of the DC-to-DC converter (L_{BST}). For stability, the inductance of the coil should remain above 0.33 μH and below 2.2 μH under all conditions. The most commonly available values are 1 μH and 1.5 μH . A nominal value 1 μH provides the optimum balance between current capability, component size and efficiency.

The choice of inductor is configured using DCCV bit. It is strongly influenced by the impedance of the haptic device used in the application. The haptic impedance determines the output current of the DC-to-DC converter. The coil current contains a ripple around the average current resulting in a peak inductor current, $I_{L(\text{peak})}$. The value of the peak inductor current is determined by the minimum required battery voltage, the boost voltage and the inductor value.

Recommend specifications for the DC-to-DC converter inductor are given in [Table 13-4](#).

Table 13-4: DC-to_DC recommended inductor

| Specification | Min | Typ | Max | Unit |
|------------------------------------|---------------------|-----|-----|------------------|
| nominal inductance; 20 % tolerance | ^[1] 0.47 | - | 2.2 | μH |
| DC resistance | - | - | 100 | $\text{m}\Omega$ |
| saturation current | - | 4.2 | - | A |

[1] 0.33 μH (min) at $I_{L(\text{peak})}$.

13.2 PCB layout considerations

When designing the PCB layout for a class-D amplifier and booster, great care must be taken circuit. The layout can affect the haptic performance, the booster performance, the electromagnetic compatibility (EMC) performance, and/or the thermal performance.

13.2.1 DC-to-DC converter stability

To avoid stability problems, the DC-to-DC converter output capacitor must be connected as close as possible to GNDB/GNDP via thick tracks. I_L must also be connected to V_{BST}/V_{DDP} in the top layer.

13.2.2 EMC considerations

EMC standards define to what degree a (sub)system is susceptible to externally imposed electromagnetic influences and to what degree a (sub)system is responsible for emitting electromagnetic signals in standby and in normal operating modes.

EMC immunity and emission values are normally measured over a frequency range from 180 kHz up to 3 GHz.

The coupling capacitors on pins V_{DD} , V_{DDP} and V_{BAT} and the booster inductor L_{BST} must be placed close to the TFA9914, referenced to a solid ground plane. The design must include a solid ground plane below the IC.

When designing a filterless class-D amplifier, long haptic cables (or traces) must be avoided. Long haptic cables have a negative effect on electromagnetic emissions. Use haptic traces/cables of less than 10 cm.

13.3 Application diagrams

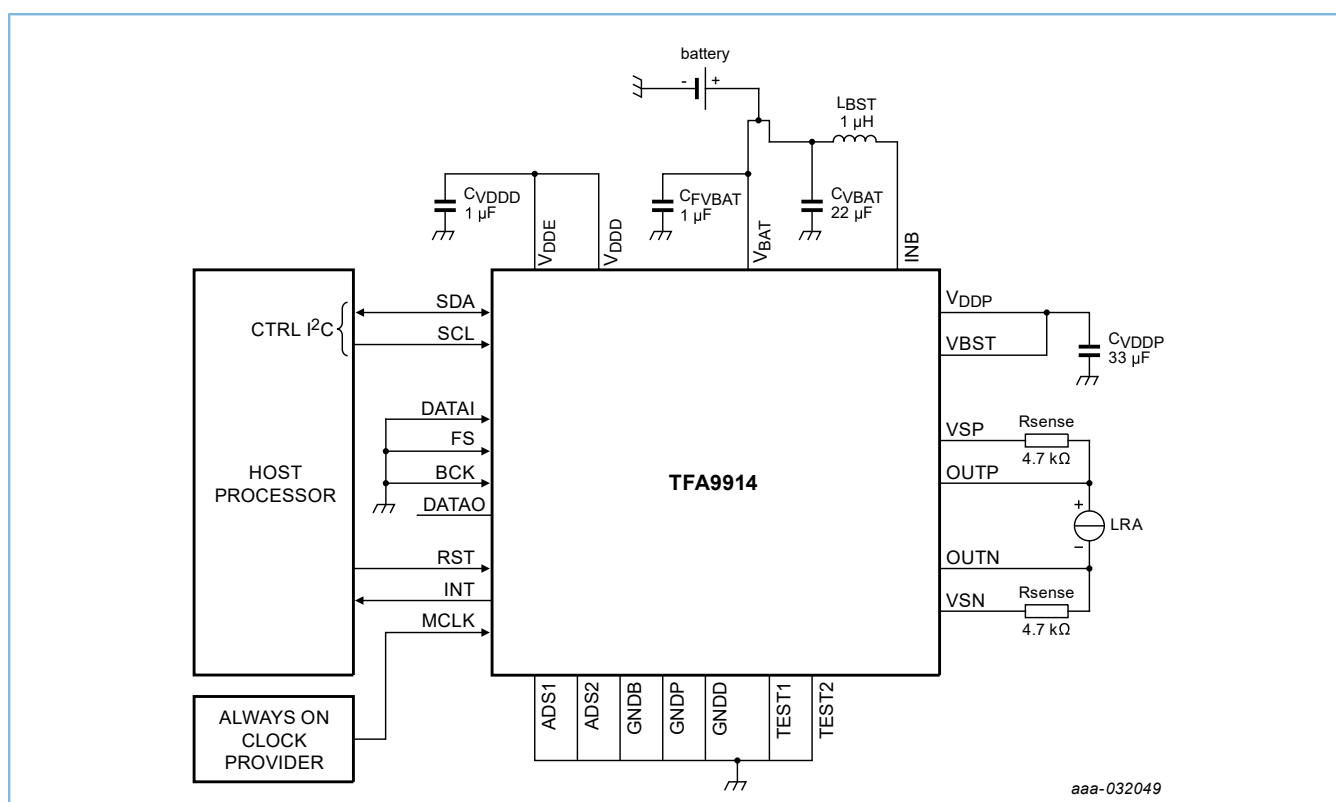


Figure 13-1: Haptic application with always-on MCLK

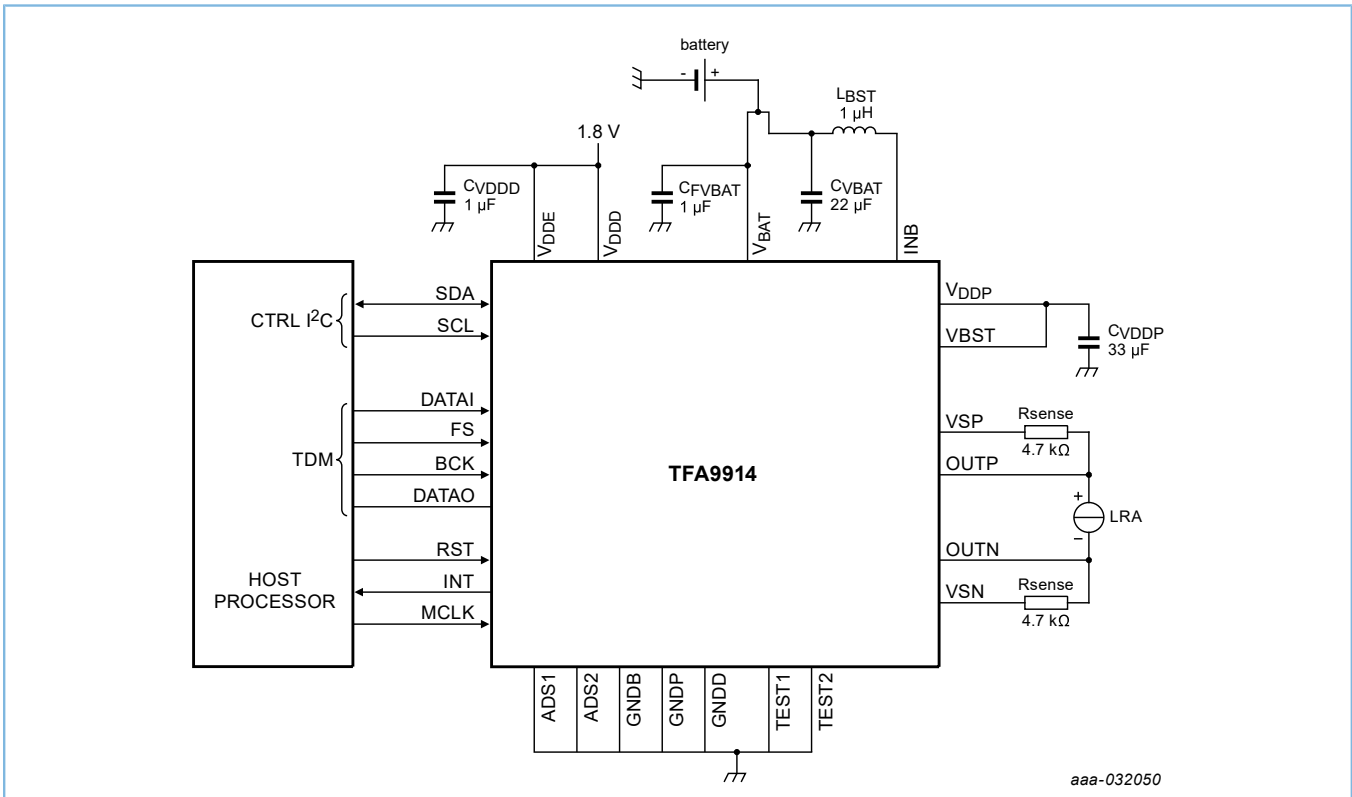


Figure 13-2: Haptic application with TDM stream

14 Package outline

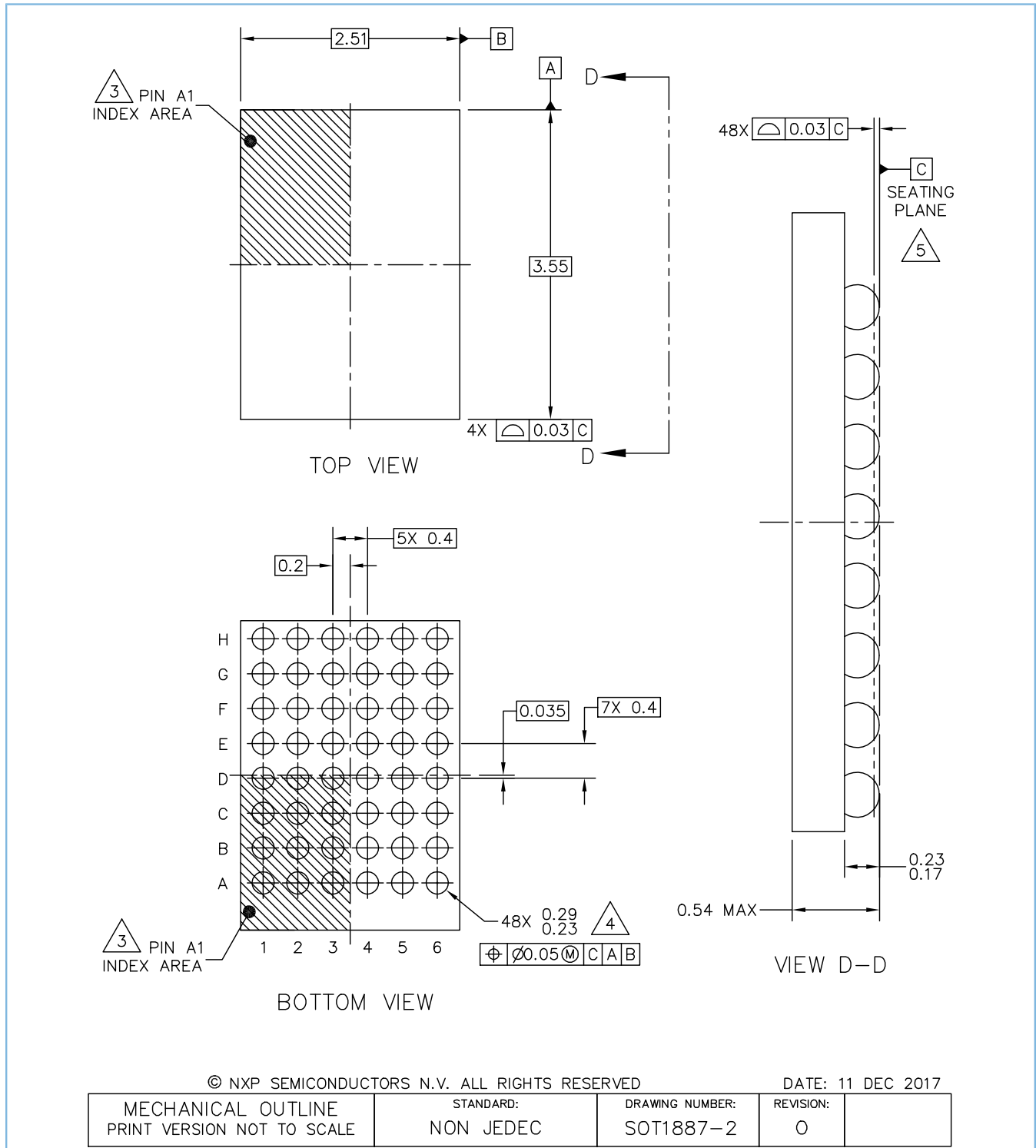


Figure 14-1: TFA9914UK package outline SOT1887-2 (WLCSP48)

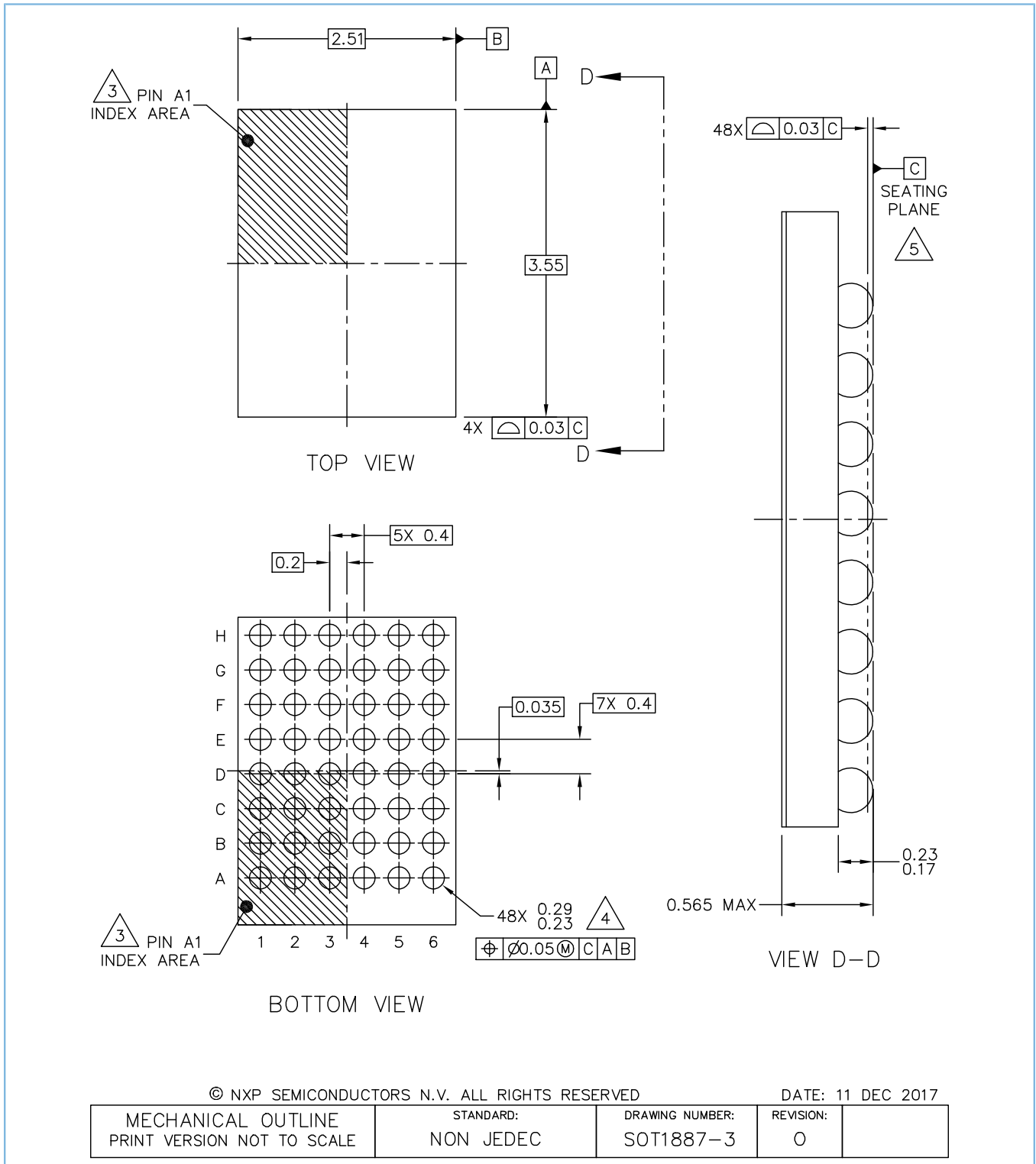


Figure 14-2: TFA9914BUK package outline SOT1887-3 (WLCSP48)

15 Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This section provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix Technology WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering
 - A lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15-1](#)) than a SnPb process, thus reducing the process window.
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board.
- Reflow temperature profile

This profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. The peak temperature must be high enough for the solder to make reliable solder joints (a solder paste characteristic) while it is low enough to not damage the packages and/or boards. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 15-1](#).

Table 15-1: Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|--------------|---------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2 000 | > 2 000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering (see [Figure 15-1](#)).

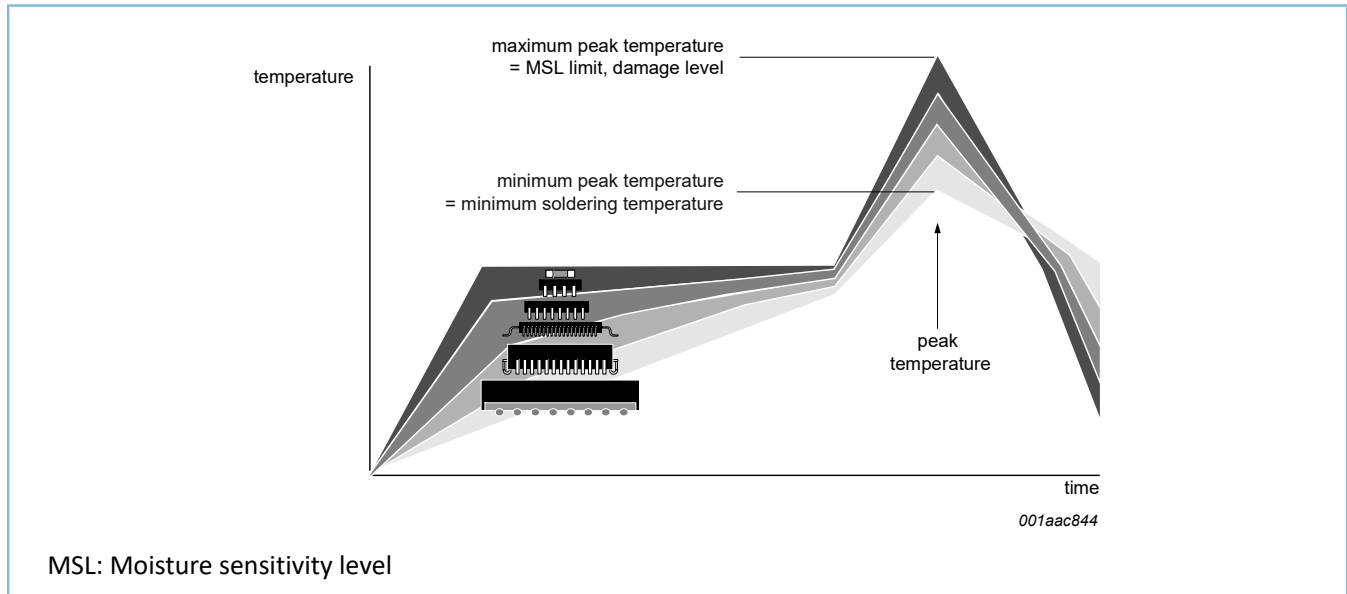


Figure 15-1: Temperature profiles

For further information on temperature profiles, see IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.1 Stand-off

The stand-off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand-off, the better the stresses are released due to thermal expansion coefficient (TEC) differences between substrate and chip.

15.3.2 Quality of solder joint

When the entire solder land has been wetted by the solder from the bump, a flip-chip joint is considered to be a good joint. The surface of the joint must be smooth and the shape symmetrical. The soldered joints on a chip must be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with a high ratio of the bump diameter to bump height, i.e. low bumps with a large diameter. No failures have been found to be related to these voids. To monitor defects such as bridging, open circuits, and voids, solder joint inspection after reflow can be done using X-ray.

15.3.3 Rework

In general, rework is not recommended. Rework is the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip are damaged. In that case, do not reuse the chip.

When the substrate is heated until it is certain that all solder joints are molten, the device can be removed. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Use plastic tweezers to remove the device, because metal tweezers can damage the silicon. The surface of the substrate must be carefully cleaned and all solder and flux residues and/or underfill must be removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16 Legal and contact information

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17 Revision history

Table 17-1: Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|--------------------------|---------------|-----------------|
| TFA9914_SDS v 2.0 | 20200121 | Product short data sheet | - | TFA9914_SDS v.1 |
| Modifications: | • Updated document format based on Goodix template | | | |
| TFA9914_SDS v.1 | 20190515 | Product short data sheet | - | - |